Supplementary Material: Prospects of Silicide Contacts for Silicon Quantum Electronic Devices

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I. PLATINUM SILICIDE CHARACTERIZATION

1. XRD

To determine the crystallinity, phase and stoichiometry of our silicide films as a function of growth temperature and time we used the X-ray diffraction (XRD) method. The measurements were done on samples annealed at 300 °C, 450 °C for 30, 60 and 300 s as well as a reference sample that was not annealed. Fig. S1(a) demonstrates typical diffraction patterns obtained at the samples of annealing time of 60 seconds at the range of diffraction angles $2\theta = 20°$ to $56°$. Intense reflexes of Si are observed in the patterns of all samples. The Pt peak present around $2\theta = 39.8°$ for the unannealed sample disappears for all annealed samples. At 300 °C the Pt pick has given its place to two picks that correspond to PtSi indicating the start of the silicidation phase. At 450 °C intense reflexes of PtSi, emerge for many diffraction angles, reflecting the crystaline formation of the PtSi. The tested annealing times of 30, 60 and 300 seconds had no significant effect on the XRD maps.

2. Kelvin Probe Force Microscopy

We measure the work function difference between the silicide samples and the intrinsic silicon using Kelvin probe force microscopy with an atomic force microscope (see Fig. S1(b))[1]. The work function difference for the PtSi annealed at a temperature of T =300 °C is in the range of 0.58-0.48 eV for an annealed time of 30, 60 and 300 s. The work-function difference drops to 0.25 eV due to silicidation for the sample annealed at 450 °C. Comparing with literature (Φ_{Pt} = 5.6 eV, Φ_{PtSi} = 4.9 - 4.98 eV and Φ_{Si} = 4.66 eV)[2] we find reasonable agreement for our silicide with the values reported elsewhere. This is indicative for nearly complete PtSi formation[3–5]. In this temperature regime an increase of anneal time does not influence the work-function.

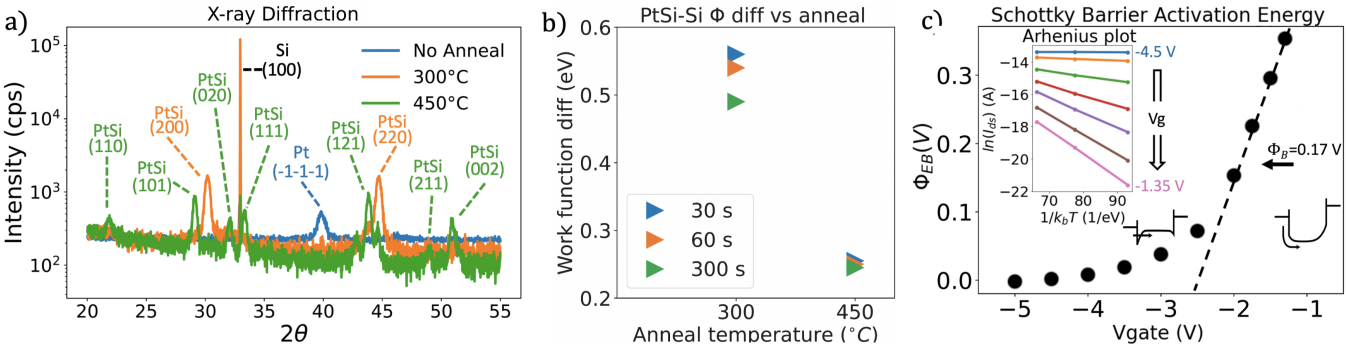

FIG. S1: a) XRD maps of counts per second in logarithmic scale for different diffraction angles of Pt silicide samples without annealing and with different annealing temperatures. PtSi peaks obtained from Crystallography open Database. Data analyzed with DIFFRAC.Eva - Bruker b) Work-function difference between intrinsic Si and PtSi as a function of annealing temperature measured with Kelvin probe force microscopy. c) Effective SB height as a function of V_g (at V_{sd} = 20 mV) for a Si MOSFET with PtSi contacts ($g_l = 9\mu m$, $f_p = 350nm$ and $f_l = 1\mu m$) extracted at temperatures from 150 K to 225 K.

3. SB height estimation

Transmission of charge carriers in devices with barriers is governed by two distinct processes: thermionic emission over the barrier and thermally assisted tunneling through the barrier. The former is dominant if the electron temperature is on the order of the barrier height and phonon energies are sufficient to lift charge carriers above the barrier. Thermally assisted tunneling through the barrier can dominate if the electron temperature is lower than the barrier height and therefore charge carriers need to tunnel through the barrier. To some extent the thermally assisted tunneling regime can be captured as thermal emission over an effective barrier, where the effective barrier height is lower than the original barrier by the thermal energy of the excited charge carriers[6,7]. In this case the source-drain current I_{SD} depends on temperature as:

$$I_{SD} \propto \exp\left(-q\Phi_{EB}/k_BT\right), \tag{S1}$$

where k_B is Boltzman's constant, q is the carrier charge, T is temperature and we omit other pre-factors as they vary much slower with temperature[8].
Additionally, for SBMOSFETs there are multiple gate voltage regimes. If the channel is off, the barrier extends over the entire channel and, unless the channel is very short, tunneling does not play a role. The only relevant transport mechanism is then thermal emission over the barrier. For holes, the highest point of the barrier is then either the Schottky barrier height given by the difference between the Fermi-energy and the valence band at the contact interface or the height of the potential in the channel. If the transistor is on, the barrier height is given by the Schottky barrier and since there are now available states in the channel, tunneling becomes a relevant transport mechanism. Here the effective barrier height deviates from the actual height of the barrier and can be lower than the Schottky barrier.
The inset in Figure S1(c) shows an Arrhenius plot, where the natural logarithm of the source-drain current I_{ds} at 20 mV source-drain bias is plotted against the inverse of thermal energy $1/k_BT$ at different gate voltages V_g. The main panel in Fig. S1(c) shows the extracted effective barrier height Φ_{EB} as a function of gate voltage V_g, that was extracted from the inset using eq.(1). At higher gate voltage the effective barrier height scales linearly with the gate voltage consistent with the regime where tunneling does not play a role. In this regime the valence band moves linearly with the gate-voltage as there is no accumulation in the channel, such that the effective barrier height is also a linear function of the gate-voltage. At lower gate-voltage we enter the thermally assisted transport regime where tunneling lowers the effective barrier. Also accumulation in the channel means that the valence band energy is no longer a linear function of the gate voltage.
We can estimate the Schottky barrier height as the height of the effective barrier at the gate voltage when it transitions from the linear to the non-linear regime. In Fig. S1(c) this gate voltage corresponds to a value of $\Phi_{SB} = 170 \pm 20\ mV$. This method may offer a mean to estimate the SB height but is limited due to contributions from thermal assisted tunneling even at the regime near the device tun-on as we discuss in the Fig. 2 of the main text.

II. DIFFERENT OXIDE STACKS

To investigate the possibility of localized states originating from the gate oxides we have fabricated devices with different oxide stacks on top of the 7 nm thermal SiO_2 that we have on every device. We vary the HfO_2 thickness and, since the trapped charge density in HfO_2 is higher than in SiO_2[9–16], we should therefore see an impact on the number of resonant features in our devices if the associated localized states are linked to trapped charges in the oxide. The first variation of the stack is a full 15 nm high-k HfO_2 stack (inset in Fig. S2(a)) which results in an earlier turn on of the device compared to the oxide stack due to a less voltage drop on the oxide. The second variation of the oxide stack is the stack from the main paper where we used HfO_2/SiO_2 4−7 nm (inset in Fig. S2(b)). The third variation of the oxide stack has no HfO_2 at all and instead only 7 nm SiO_2 (ALD) on the thermal SiO_2. In the first generation of those devices we found leakage from the PtSi contact to the gate, which we attribute to Pt contamination of the silicon oxide as previously observed by others[17]. We mitigate the leakage using a 5 nm Ti cap around the silicide above the substrate, which acts as a diffusion barrier and prevents leakage (Fig. S2(c)). The drawback of this diffusion barrier is increased screening of the gate electric field at the contact due to Ti covering the sidewalls of the PtSi on the surface. This results in lower currents due to wider Schottky barriers.

Figure S2 shows conductance maps of characteristic devices for each stack. While the turn-on of the devices shifts in agreement with the efficiency of SB tuning and the screening from the Ti cap as discussed above, we find a large number of resonant features for all oxide stacks. In the stacks with HfO_2 there is no clear difference in the density of the resonant features. For the stack with SiO_2 the overall conductance is lower due to the increased screening, but the resonant features are still clearly visible. This indicates that the resonant transport features in our devices are not linked to oxide traps, but to other types of impurities or defects in the barriers.
Note that the fabrication of the devices involves lift-off of the Pt, followed by a thorough cleaning step with piranha acid as well as etching of a global metallic layer to form a gate-electrode that overlaps the contact. We therefore do not expect etch damage or

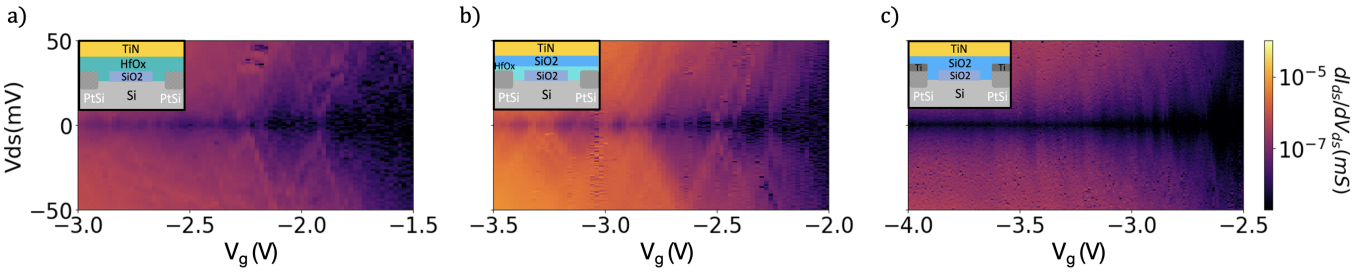

FIG. S2: Conductance as a function of gate voltage V_g and source-drain bias V_{ds} in 3 devices with different gate oxides. a) SiO_2/HfO_2 (7/4 nm), b) HfO_2 (15 nm) and c) SiO_2 (7 nm)

resist residues in the contact regions at the interface of the PtSi and the channel This excludes another possibility for the creation of localized states. Together with the lever arm discussion and the results from devices with doped contacts, we conclude that the localized states are instead linked to metallic charge islands in the SBs.

III. CONTACT MATERIAL

We also fabricated similar SBMOSFETs with NiSi contacts using the same process flow as for the SBMOSFETs with PtSi contacts. For the silicide formation, the samples were annealed at 400°C for 1 min. Similar to the diffusion barrier in the PtSi SBMOSFETs with pure SiO_2, we employ a 5nm titanium cap on top of the Ni to prevent diffusion in the SiO_2. Figure S3(a,b) shows the differential conductance for the NiSi devices as a function of gate-voltage and bias-voltage. The Fermi energy in NiSi is positioned in the middle of the gap of the Silicon, which creates a larger Schottky barrier of 0.48 eV to the valence band but allows for ambipolar operation. We observe resonant transport features for both electrons and holes, with the electrons consistently displaying fewer resonances per gate-voltage.

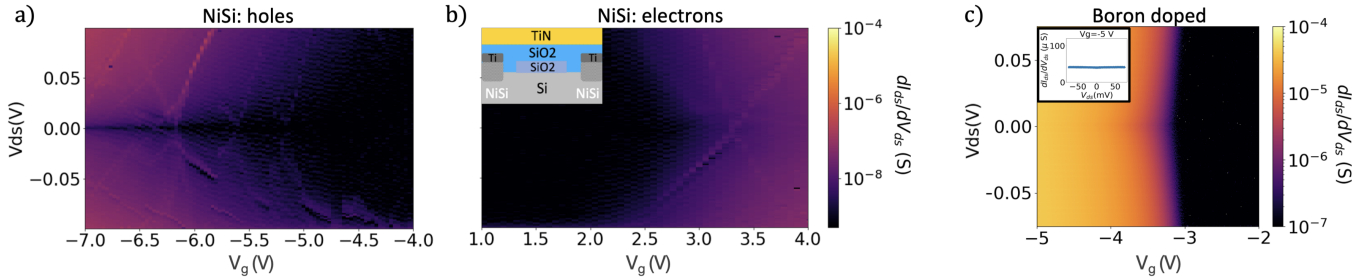

FIG. S3: Differential conductance as a function of gate-voltage V_{gate} and bias-voltage V_{ds} in SBMOSFET with NiSi contacts at 4 K. (a) Negative gate voltages for a hole channel. (b) Positive gate voltages for an electron channel. Inset: Schematic of the material stack. (c) Differential conductance as a function of gate-voltage V_g and source-drain bias V_{ds} in a MOSFET with of a doped contacts at 4 K. (Inset) Linecut in the low source-drain bias regime at $V_g = -5$ V with no signature of transport through a Schottky barrier or localized states.

IV. DOPED CONTACTS

Unlike the devices in the main text, the contacts in these devices were fabricated using Boron-doped poly-Silicon from low-pressure chemical vapor deposition. The dopants were then activated at 900°C for 1 minute before the device was finished following a similar process flow to the devices discussed in the main text. Figure S3(c) shows the differential conductance in such a device as a function of gate-voltage V_g and source-drain bias-voltage V_{ds}. In this device there is no sign of a non-linearity around zero source-drain bias and also no sign of transport through localized states. This indicates a clean, ohmic contact and confirms that the resonant features in our SBMOSFETs are related to localized states in the barriers, not in the channel.

V. LEVER ARM CALCULATION

We first derive a formula for the lever arm of a state that is pinned to the valence band. At cryogenic temperatures the Fermi distribution is approximately a step function around the source/drain chemical potential. Assuming a constant density of states for small changes in energy in two-dimensions, a small difference in charge density in the accumulated channel can then be approximated as:

$$\Delta n_{2D} = \Delta E_V \cdot DOS_{2D}, \tag{S2}$$

where ΔE_V is the distance from the valence band to the chemical potential in source and drain, DOS_{2D} is the 2 dimensional density of states and n_{2D} is the charge density in the channel. We can also calculate a change in charge density using a parallel plate capacitor model as:

$$\Delta Q_{ch} = C \cdot \Delta V_g \Rightarrow \Delta n_{2D} \cdot A \cdot e = \frac{A \cdot \varepsilon_{SiO_2}}{d_{ox}} \cdot \Delta V_g \tag{S3}$$

By dividing eq.(2) with eq.(3) we can calculate the lever arm of the gate to the valence band via:

$$\alpha_{gv} = \Delta E_V / \Delta V_g = \varepsilon_{SiO_2} \frac{\pi \hbar^2}{m_h d_{\mathrm{ox}} e}, \tag{S4}$$

where m_h is the effective mass for heavy holes in silicon, d_{ox} the effective SiO_2 thickness and ε_{SiO_2} is the SiO_2 and vacuum permittivity respectively. For $m_h = 0.49 m_0$ and d_{ox}= 16 nm we obtain $\alpha_{gv} = 7.5$ meV/V.

Next we compare this to the lever arms of the resonant features in our data. We therefore extracted the lever arms from

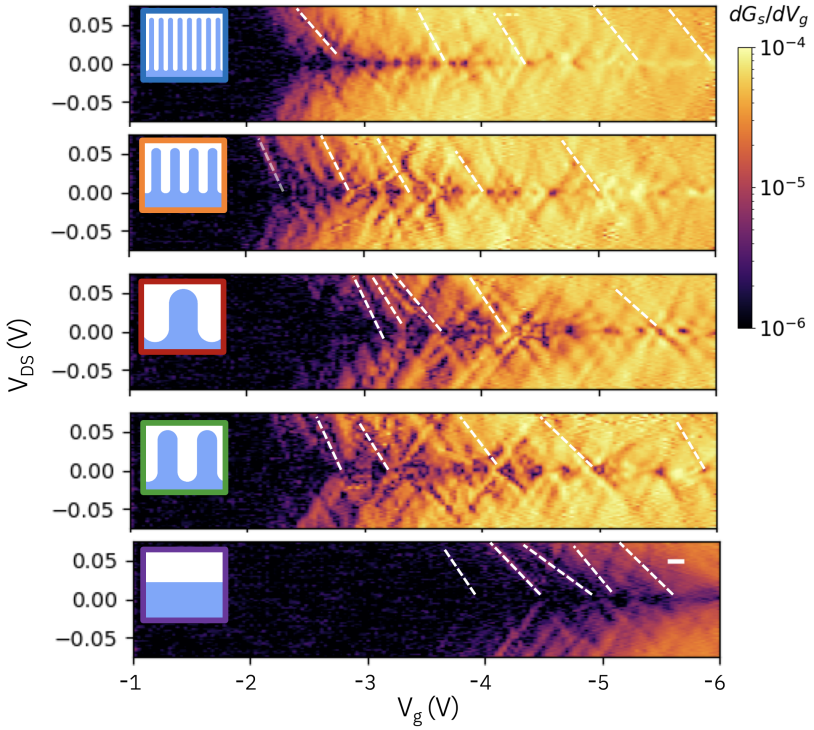

FIG. S4: Derivative of the conductance with respect to V_g as a function of V_g and V_{ds} in 5 devices with different contact geometries.

measurements for all 5 variation of the meanders shown in Fig.S4. The results are summarized in the table in Fig. S5.

In the work of of Clavet et al.[18,19] lever arms of 450 meV/V were extracted for an oxide thickness of 3.4 nm leading to a similar lever arm per oxide thickness as in our devices.

α_{gl}(meV /V)

				
75	120	170	180	110
90	120	90	160	160
60	70	11	190	160
100	100	80	90	90
90	70	90	110	90

FIG. S5: Values of lever arms (α_{gl}) from the data in Fig. S4.

REFERENCES

[1] N. Torkhov and V. Novikov, "Kelvin probe force microscopy study of the electrostatic system of the crystal surface of AuNi/GaN Schottky diodes," Semiconductors **54**, 337–344 (2020).

[2] T. J. Drummond, "Work functions of the transition metals and metal silicides," Tech. Rep. (Sandia National Lab.(SNL-NM), Albuquerque, NM (United States), 1999).

[3] M. K. Niranjan, S. Zollner, L. Kleinman, and A. A. Demkov, "Theoretical investigation of PtSi surface energies and work functions," Phys. Rev. B **73**, 195332 (2006).

[4] S. M. Sze, Y. Li, and K. K. Ng, *Physics of semiconductor devices* (John wiley & sons, 2021).

[5] J. P. Snyder, C. Helms, and Y. Nishi, "Experimental investigation of a PtSi source and drain field emission transistor," Applied physics letters **67**, 1420–1422 (1995).

[6] J. M. Larson and J. P. Snyder, "Overview and status of metal s/d Schottky-barrier MOSFET technology," IEEE Transactions on Electron Devices **53**, 1048–1058 (2006).

[7] I. Bejenari, M. Schröter, and M. Claus, "Analytical drain current model of 1-D ballistic Schottky-barrier transistors," IEEE Transactions on Electron Devices **64**, 3904–3911 (2017).

[8] S. Das, H.-Y. Chen, A. V. Penumatcha, and J. Appenzeller, "High performance multilayer MoS_2 transistors with scandium contacts," Nano letters **13**, 100–105 (2013).

[9] D. Winslow, J. Johnson, and C. Williams, "Nanometer scale study of HfO_2 trap states using single electron tunneling force spectroscopy," Applied Physics Letters **98**, 172903 (2011).

[10] M. Martínez-Puente, P. Horley, F. Aguirre-Tostado, J. López-Medina, H. Borbón-Nuñez, H. Tiznado, A. Susarrey-Arce, and E. Martínez-Guerra, "Ald and peald deposition of hfo2 and its effects on the nature of oxygen vacancies," Materials Science and Engineering: B **285**, 115964 (2022).

[11] F. Caruso, P. La Torraca, L. Larcher, G. Tallarida, and S. Spiga, "The electrons' journey in thick metal oxides," Applied Physics Letters **121**, 012902 (2022).

[12] D. M. Ramo, J. Gavartin, A. Shluger, and G. Bersuker, "Spectroscopic properties of oxygen vacancies in monoclinic HfO_2 calculated with periodic and embedded cluster density functional theory," Physical Review B **75**, 205336 (2007).

[13] P. Broqvist and A. Pasquarello, "Oxygen vacancy in monoclinic HfO_2: A consistent interpretation of trap assisted conduction, direct electron injection, and optical absorption experiments," Applied physics letters **89**, 262904 (2006).

[14] Y.-Y. Liu, F. Liu, R. Wang, J.-W. Luo, X. Jiang, R. Huang, S.-S. Li, and L.-W. Wang, "Characterizing the charge trapping across crystalline and amorphous Si/SiO2/HfO_2 stacks from first-principle calculations," Physical Review Applied **12**, 064012 (2019).

[15] A. Kerber and E. A. Cartier, "Reliability challenges for cmos technology qualifications with hafnium oxide/titanium nitride gate stacks," IEEE Transactions on Device and Materials Reliability **9**, 147–162 (2009).

[16] J. Strand, P. La Torraca, A. Padovani, L. Larcher, and A. L. Shluger, "Dielectric breakdown in HfO_2 dielectrics: Using multiscale modeling to identify the critical physical processes involved in oxide degradation," Journal of Applied Physics **131**, 234501 (2022).

[17] B. D. B. Deng, C. S. C. Shu, and H. K. H. Kuwano, "Improvement of electrical characteristics of Pt-diffused devices," Japanese journal of applied physics **34**, 2969 (1995).

[18] L. Calvet, J. Snyder, and W. Wernsdorfer, "Excited-state spectroscopy of single Pt atoms in Si," Physical Review B **78**, 195309 (2008).

[19] L. Calvet, W. Wernsdorfer, J. Snyder, and M. Reed, "Transport spectroscopy of single Pt impurities in silicon using Schottky barrier MOSFETs," Journal of Physics: Condensed Matter **20**, 374125 (2008).