

Ambipolar quantum dots in undoped silicon fin field-effect transistors

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We integrate ambipolar quantum dots in silicon fin field-effect transistors using exclusively standard complementary metal-oxide-semiconductor fabrication techniques. We realize ambipolarity by replacing conventional highly-doped source and drain electrodes by a metallic nickel silicide with Fermi level close to the silicon mid-gap position. Such devices operate in a dual mode, either as classical field-effect or single-electron transistor. We implement a classical logic NOT gate at low temperature by tuning two interconnected transistors into opposite polarities. In the quantum regime, we demonstrate stable quantum dot operation in the few charge carrier Coulomb blockade regime for both electrons and holes.

Quantum information can be encoded in the spin state of a single electron or hole confined to a semiconductor quantum dot (QD)^{1–3}. Several material systems have been explored in the search of a highly coherent spin quantum bit (qubit). Silicon (Si) is a particularly promising material platform for scalable spin-based quantum computing because of its fully developed, industrial manufacturing processes, which enable reliable and reproducible fabrication at the nanometer scale^{4–6}. Furthermore, natural silicon consists of 95% non-magnetic nuclei (92% ²⁸Si, 3% ³⁰Si), suppressing hyperfine-induced decoherence^{7–9}. A nearly nuclear-spin-free environment can additionally be engineered by means of isotopic purification¹⁰. Electron spins in silicon are also subject to a weak spin-orbit interaction (SOI) and can thus be almost completely isolated from environmental noise¹¹. As a result, an excellent dephasing time T_2^* of 120 μ s has been demonstrated for the electron spin qubit in isotopically enriched silicon ($\geq 99.9\%$ of ²⁸Si)⁵.

For scalable quantum circuits, qubit control via electric rather than magnetic fields is more promising in terms of speed and hardware implementation. In this regard, the hole spin represents an attractive alternative to its electron counterpart^{12–14}. The asymmetry of the silicon band structure with respect to the conduction (CB) and valence bands (VB) manifests itself in different characteristics for electrons and holes. While the electron Bloch function has s-wave symmetry, the hole has p-wave symmetry. Consequently, hole spins experience a weaker hyperfine, yet stronger SOI, which enables fast, all-electrical spin manipulation^{15–17}. Despite these potential benefits, hole spin qubits in silicon are still largely unexplored. Recently, qubit functionality with fast, purely electrical, two-axis control was shown for a hole spin, yet with inferior coherence compared to the electron spin⁶.

Usually, either electrons^{18–21} or holes^{6,17,22–24} are confined in silicon QDs. Ambipolar devices, by contrast, can be operated in both the electron and hole regime^{25–32}. For planar silicon metal-oxide-semiconductor (MOS) QD structures, ambipolar behavior was demonstrated by integrating both *n*- and *p*-type reservoirs on the same device^{33–37}. Ambipolar devices provide great flexibility for scalable spin-based quantum circuits, since both types of

charge carriers can be manipulated in exactly the same crystalline environment, allowing for direct benchmarking of hole against electron spin qubits.

Here, we report on a new generation of ambipolar silicon QD devices based on today's industry standard, non-planar fin field-effect transistors (FinFETs)^{38–40}. In an overlapping-gate structure, ambipolarity is achieved by using a metallic nickel silicide (NiSi) with Fermi energy close to the silicon mid-gap for source (S) and drain (D) electrodes^{27,28,41}. This approach allows for a highly compact device layout, is easy to integrate and fully compatible with complementary metal-oxide-semiconductor

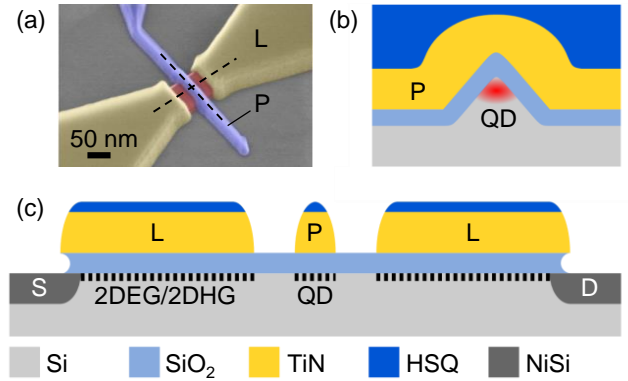


FIG. 1. Device layout: (a) False-color scanning electron micrograph showing a FinFET structure before sealing it with a SiO_2 passivation layer. Devices consist of a single plunger (blueish color) and two lead gates (yellowish color) to silicided source and drain. The gate electrodes are operated in accumulation mode and are wrapped around the silicon fin (reddish color) defining the transistor channel. The dashed lines indicate the orientation of the schematic cross sections perpendicular to (b) and along (c) the fin. For a positive (negative) gate voltage electrons (holes) are accumulated at the Si-SiO₂ interface below the electrode. While the lead gates are designed to induce a two-dimensional electron (hole) gas opening low-resistance leads to source and drain, the plunger gate allows for local electrostatic control of the channel and to create a QD, which is located at the apex of the triangular shaped fin.

(CMOS) technology. We successfully operate the devices both in a classical and quantum mode⁴², demonstrating simple co-integration between silicon-based qubits and traditional CMOS control hardware.

The layout of the home-built devices is shown in Fig. 1. First, the fin structures are defined on a near-intrinsic silicon substrate ($\rho > 5000 \Omega\text{cm}$, (100) surface) by means of electron-beam lithography (EBL) and dry etching, yielding a fin height of $\simeq 25 \text{ nm}$. A sacrificial thermally grown silicon dioxide (SiO_2) layer, which is removed in buffered hydrofluoric acid, allows for narrowing of the fin width ($\gtrsim 10 \text{ nm}$) and cleaning of etch-induced surface damage. This procedure leads to an almost triangular cross section for the narrowest fins. Subsequently, the gate stack is deposited, consisting of a high-quality, thermally grown SiO_2 layer ($\sim 10 \text{ nm}$, breakdown voltage $\sim 10 \text{ V}$), covered by 40 nm of titanium nitride (TiN). An uniform layer of TiN, which is wrapped around the silicon channel, is obtained by atomic layer deposition. The gate layer is patterned by means of EBL and dry etching of TiN, resulting in a gate length of $\gtrsim 25 \text{ nm}$ at a gate-to-gate separation of $\gtrsim 50 \text{ nm}$. Conventional impurity-doped source and drain electrodes are replaced by a metallic, non-magnetic NiSi, forming a Schottky barrier at the S/D-to-substrate junction^{41,43}. By choosing a mid-gap silicide, ambipolar operation is realized in a simple, highly compact design, as no complementary charge reservoirs are required. So far, ambipolar silicon QDs have only been implemented by integrating separate n - and p -type contacts to the same channel, enlarging the device's footprint³³⁻³⁷. The NiSi electrodes are formed by EBL, Ni evaporation, lift-off and low-temperature silicidation annealing at 475°C for 30 min in an argon ambient. Lateral Ni diffusion below the gates allows for tuning of the Schottky barrier width, and ensures that source and drain contacts operate in an ohmic regime. After silicidation, unreacted Ni is selectively removed in order to avoid any magnetic impurities to be present in the device. Finally, the devices are protected from contamination by a SiO_2 passivation layer and are accessed via tungsten interconnects.

The data presented here is obtained from direct current electrical transport measurements with the sample cooled to $T \simeq 1.5 \text{ K}$. The devices' gate layer consists of a central plunger (P) and individual lead (L) gates to source and drain electrodes, as shown in Fig. 1 (c). The gates are operated in accumulation mode: for a negative (positive) applied voltage holes (electrons) are accumulated at the Si-SiO₂ interface. Therefore, a two-dimensional electron (2DEG) or hole gas (2DHG) forms beneath the lead gates, acting as electrostatically defined source and drain, while the plunger gate induces a Coulomb island that defines the QD. The gaps separating lead and plunger gates create tunnel barriers between them⁴⁴.

First, the devices are operated in a classical field-effect transistor (FET)-like regime. Ambipolar transistor turn-on curves, revealing both n - and p -type conduction, are presented in Figs. 2 (a), (b). The linear conductance G is plotted versus plunger gate voltage V_P at a constant lead

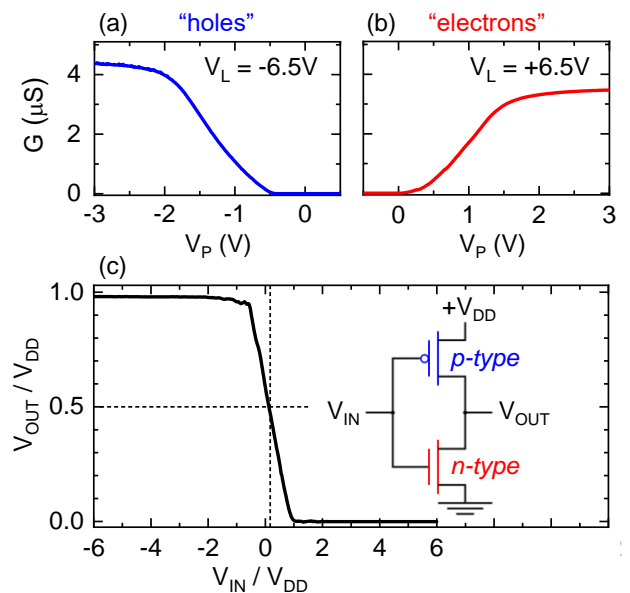


FIG. 2. Ambipolar turn-on curves and CMOS logic at cryogenic temperatures: conductance G versus plunger gate voltage V_P for the hole (a) and electron (b) regime. The lead voltage V_L is kept fixed at a value well above threshold, and the source-drain voltage V_{SD} is -1 V for holes and $+1 \text{ V}$ for electrons, where the bias polarity is chosen such that electrical stress on the device is minimized. (c) Voltage transfer characteristics and the corresponding circuit diagram of a CMOS inverter, consisting of a p -type and a complementary n -type FinFET. For *low* input $V_{\text{IN}} < 0 \text{ V}$ the output V_{OUT} is *high* and vice versa. All the measurements are performed at $T = 1.5 \text{ K}$.

gate voltage V_L of $\pm 6.5 \text{ V}$, creating conducting channels beneath the lead gates. A large source-drain voltage V_{SD} of $\pm 1 \text{ V}$ ensures that the current is not dominated by charge carrier tunneling processes. The measurement reveals a slight asymmetry in current-onset voltages with respect to zero for electrons and holes: for $V_P \gtrsim 0 \text{ V}$ n -type and for $V_P \lesssim -0.35 \text{ V}$ p -type conduction occurs. In between, the Fermi level lies in the band gap of silicon and no states are available for transport. This asymmetry is not fully understood and most likely a combination of various effects, such as a residual wafer background doping, charge traps or the metal gate work function^{34,36,37}. The lower saturation current for electrons may also be due to an asymmetry of the silicide Schottky barrier for electrons and holes.

Any CMOS circuit can in principle be constructed using ambipolar transistors as sole building blocks. In the inset of Fig. 2 (c) the most basic logic circuit - the CMOS inverter - is shown schematically. It consists of two complementary transistors connected at the gate and drain terminals. The inverter output voltage V_{OUT} is taken from the common drain electrode and is limited to the supply voltage V_{DD} , which is applied to the p -type transistor's source contact. The voltage transfer curve of our home-built inverter is presented in Fig. 2 (c). As the in-

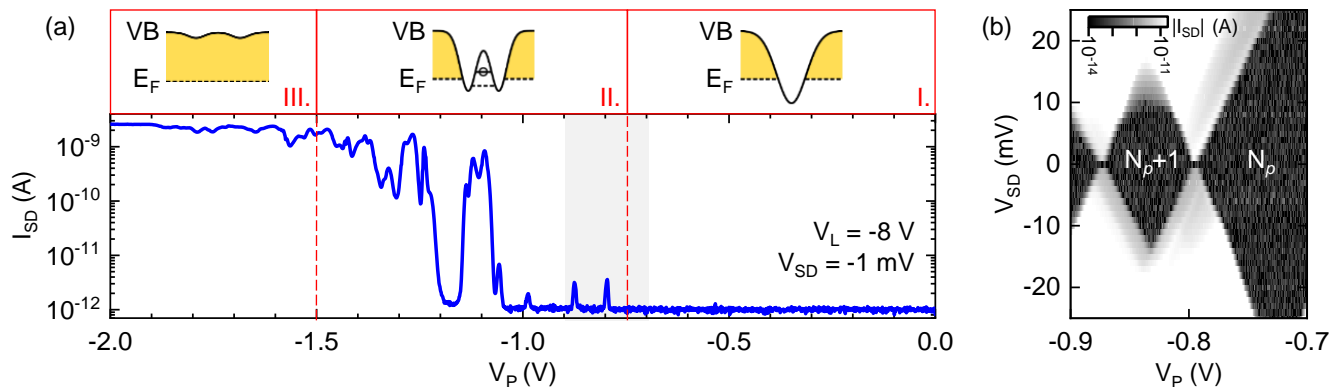


FIG. 3. QD formation: (a) source-drain current I_{SD} versus plunger gate voltage V_P in the low-bias regime ($V_{SD} = -1$ mV) on the hole side ($V_L = -8$ V). Top panel: Sketches of the real space band alignment in the vicinity of the plunger gate for the observed three different conductance regimes. (b) Charge stability map of the first measurable Coulomb resonance. The corresponding plunger gate voltage range is indicated by the grey shaded area in (a). The Coulomb diamonds are labeled with the number of holes residing on the dot ($N_p \gtrsim 0$). All the measurements are performed at $T = 1.5$ K.

put voltage V_{IN} is varied from *low* to *high*, the inverted input signal is measured at the output, going from *high* to *low*. The *high* output level gets with $0.98 V_{DD}$ close to the ideal limit. The transition zone, however, is centered around $V_{IN} \simeq 0.15 V_{DD}$ and not $V_{DD}/2$ as the devices are not perfectly matched in threshold voltage and amplification. Nevertheless, the successful operation of an inverter at low-temperature proves that classical CMOS logic can be performed.

In the linear transport regime at $V_{SD} = -1$ mV, quantum confinement in an island, which forms below the plunger gate, gives rise to pronounced Coulomb oscillations. The plunger gate-dependent source-drain current I_{SD} at $V_L = -8$ V is shown in Fig. 3 (a). In this regime the current is dominated by hole tunneling. The measurement is performed on a device with a fin width of $\simeq 20$ nm, plunger gate length of $\simeq 25$ nm and plunger-to-lead-gate separation of $\simeq 25$ nm. Three different regimes of hole transport, which are depicted schematically in the top panel of Fig. 3 (a), are observed: (i) for $V_P \gtrsim -0.8$ V the barrier induced by the plunger gate prevents current flow. (ii) For $V_P \lesssim -0.8$ V a series of Coulomb resonances indicates single-hole tunneling via a QD formed beneath the plunger gate. In the valleys between the peaks the device operates in Coulomb blockade, i.e. the QD contains a fixed number of holes^{3,4}. As this number increases with more negative V_P , the plunger gate's fringe fields lower the barriers and the QD starts to open ($V_P \lesssim -1.05$ V). (iii) For $V_P \lesssim -1.5$ V a conducting channel is opened and the current is limited by the series resistance of the device. Similar behavior is found for positive V_P on the electron side (see Fig. 4).

The first measurable Coulomb resonances are investigated in more detail by means of bias spectroscopy. In Fig. 3 (b) the charge stability diagram is shown for a plunger gate voltage range highlighted by the gray shaded area in Fig. 3 (a). Within this range, the tunnel barriers are still well defined. Clear Coulomb diamonds with a

fixed number of holes N_p on the QD are observed. Outside the diamonds sequential tunneling of holes through the QD occurs. The small dimensions of the device and the closing of the Coulomb diamonds at zero bias suggest formation of a single QD. Moreover, similar coupling of the QD to both source and drain (from the shape of the diamond we determine that the source and drain lever arms differ by just $\sim 6\%$) dictates a central location of the charge island below the plunger gate. The charging energy is determined to be $e^2/C_\Sigma \simeq 16$ meV that corresponds to a total capacitance C_Σ of 10 aF. The plunger gate voltage spacing of the Coulomb resonances yields a gate capacitance C_g of 2.1 aF. The latter is in good agreement with the calculated MOS plunger gate capacitance, which can be estimated by an equivalent planar capacitor $C_g = \epsilon_0 \epsilon_{SiO_2} S / t_{SiO_2} \sim 3.5$ aF with $\epsilon_{SiO_2} = 3.9$ the dielectric constant, t_{SiO_2} the oxide thickness and S the surface area of the gate-fin overlap. The gate voltage lever arm is $\alpha = C_g / C_\Sigma \simeq 0.21$. The large charging energy and the wide opening in V_{SD} of the last diamond could indicate that the device is operating in the single-hole regime. However, more sensitive charge detection methods and a device structure that offers more tunability are necessary to evaluate this^{3,45}. The lines of increased conductance that run parallel to the diamond edges in Fig. 3 (b) can be attributed to resonant tunneling processes⁴⁶, for instance excited orbital states of the QD. Various devices have been measured, showing similar behavior and charging energies. However, instabilities and deviations from the ideal picture reveal that the device performance is affected by charge-trapping defects.

Ambipolar behavior in the low V_{SD} regime is demonstrated in Fig. 4 where I_{SD} is plotted versus V_P for both the electron and hole regime. The data was measured on a different device with the same physical dimensions as the one of Fig. 3 (the electron regime of this device suffers from charge traps). Both in the electron and hole transport regime Coulomb oscillations occur. However, the

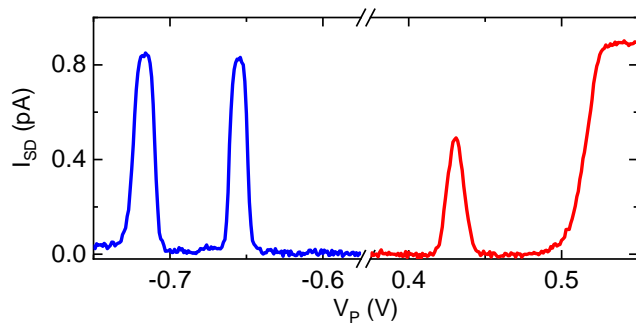


FIG. 4. Ambipolar Coulomb blockade: source-drain current I_{SD} versus plunger gate voltage V_P for holes (blue, $V_L = -4$ V, $V_{SD} = +0.5$ mV) and electrons (red, $V_L = +3.2$ V, $V_{SD} = +2.5$ mV). The measurements are performed at $T = 1.5$ K.

asymmetry in the band structure of silicon with respect to the conduction and valence bands manifests itself in asymmetric electrical transport characteristics for holes and electrons. While for electrons a single current peak exists before the barriers vanish, the hole side exhibits a similar behavior to the previous device with several Coulomb oscillations.

In conclusion, we have introduced a novel type of ambipolar silicon QDs, integrated in today's industry standard, non-planar FinFETs. By making use of a mid-gap silicide, ambipolar devices are realized with the footprint of unipolar structures. We successfully operate these devices in a classical as well as quantum mode, thus demonstrate the compatibility of silicon-based quantum circuits with traditional CMOS control hardware. Future devices with even smaller physical dimensions, improved charge noise performance and a second gate layer for in-situ adjustment of the tunnel coupling will probably allow us to reliably access the single-electron (hole) regime. Such devices will enable direct benchmarking of electron against hole spin qubits. Moreover, an interconnected array of ambipolar QDs will offer a blank canvas for building custom, on-the-fly reconfigurable “quantum CMOS” circuits, which in analogy to classical CMOS, utilize both n - and p -type devices.

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