completed, is is energetically more favorable to continue growth with island formation. Experimental studies as well as theoretical considerations have demonstrated that strain does not cause, as one might assume, dislocations inside the dots; rather, the substrate gets elastically strained as well. [Eaglesham1990]. Such islands , e.g. InAs grown on GaAs are typically of pyramidal shape and have very homogeneous size distributions; the size variances are of the order of 10% only [Leonard1993]. Since their sizes are in the range of 20 nm in width and a few nanometers in height[1], strong quantization effects can be expected inside, and have in fact been observed in many experiments, some of which we will discuss later on. Therefore, they are referred to as *self-assembled quantum dots (SAQDs)*. In some systems, the SAQDs even align with each other and form lattices of various dimensions. A three-dimensional SAQD superlattice is the topic of [P 4.2]. Here, we look at growth of linear chains of InAs SAQD islands, embedded in GaAs, Fig. 4.7. In this example, the strain in the GaAs induced by the buried InAs islands modulates the GaAs surface energy, and thus the freshly offered InAs will preferentially form dots at locations where the lattice mismatch is minimum, which is above the locations of the SAQDs next to the surface. Clearly, the spacing between adjacent InAs layers can be optimized for maximum probability of SAQD alignment. For large distances, the strain modulation at the surface becomes too weak, while for very small spacings, neighboring points of extremal strain begin to overlap.

A very different process for fabricating a layered structure is thermal oxidation of Si. For growing oxides used in electronic applications, the technique of choice is usually *dry oxidation*. The Si wafer is placed in a furnace at a temperature of about 1000 °C and exposed to oxygen. Via the reaction $Si + O_2 \to SiO_2$, the wafer oxidizes. The oxygen diffuses through the already grown oxide layer and reacts with the Si at the Si/SiO_2 interface. The oxide growth rate therefore drops as its thickness increases. Furthermore, the oxide penetrates into the Si. About 50% of the oxide layer is located below the original wafer surface. Breakdown electric fields for oxides grown with this technique can be of the order of $5 \cdot 10^8$ V/m, and are thus well suited for electronic applications.

4.1.3 Lateral patterning

The special MBE techniques CEO and SAQD growth are by no means standard technology. It is more usual to grow a heterostructure with two-dimensional translation invariance parallel to the surface, and pattern the nanostructure subsequently by some sort of lateral processing. Examples for typical sequences of process steps are given in Fig. 4.8. Column (a) is typical for many Si fabrication steps. The substrate is covered with a homogeneous metal layer, which is subsequently coated with a suitable resist. Illumination and development of the resist through a mask exposes some areas of the metal layer, while others are protected by the resist. The illumination is usually carried out with ultraviolet light or with electrons. An etch step follows, which selectively removes the free metal surfaces. here, the resist acts as an etch mask. Finally, the resist gets removed, and a patterned metal layer on the substrate results. This technique is rarely ever used in GaAs processing, since essentially all suitable metal etchants attack GaAs as well. Therefore, fabrication scheme (b) is typically used. Here, the substrate is first covered by resist, which gets illuminated and developed. Now, the metal is

[1] This is below the resolution limit of lithographic techniques, as we will see shortly.

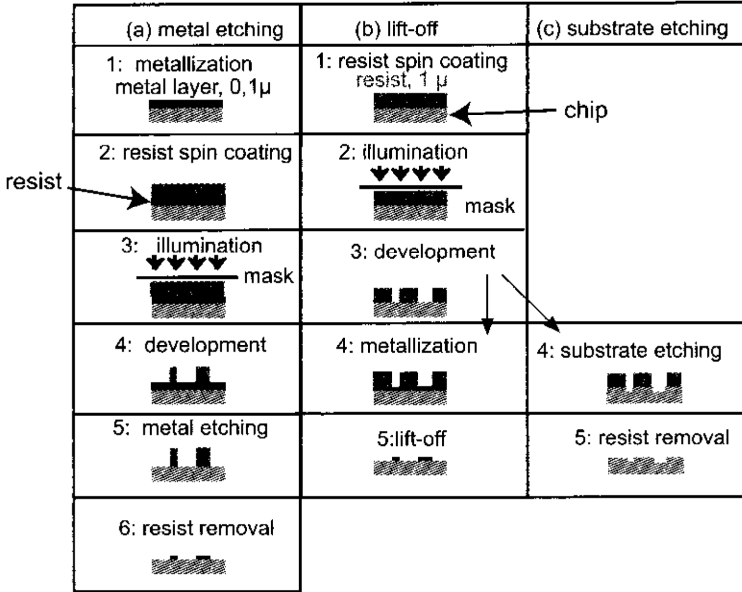

Figure 4.8: Comparison of different lateral patterning schemes for semiconductors.

evaporated on the substrate, with the patterned resist acting as evaporation mask. The *lift-off* step follows, i.e., the resist is removed with the metal film on top. The final result is identical to that one of scheme (a). For selective etching of the substrate (c), steps 1 to 3 are identical to (b). Then, the patterned resist is used as an etch mask for the substrate. We now discuss these fabrication steps in further detail.

Defining patterns in resists

The two standard techniques for imposing a pattern into a resist are optical lithography and electron beam lithography.

1. Optical lithography

   By this we mean illumination of a photoresist by visible or ultraviolet light. The sample is coated with a thin and homogeneous photosensitive resist. This is done by dropping some resist solution onto the sample, which is then rotated for about one minute at high speed, typically a few thousand rpm. The spinning speed and the viscosity of the solution determine the thickness of the resist layer, which is of the order of 1 micron.

   After baking the resist, the sample is mounted into a mask aligner, a device designed for adjusting the sample with respect to a mask that contains the structure to be illuminated. The mask aligner is equipped with a strong light source that illuminates the resist film through the mask, see Fig. 4.9. The pattern sizes are Doppler limited, which means

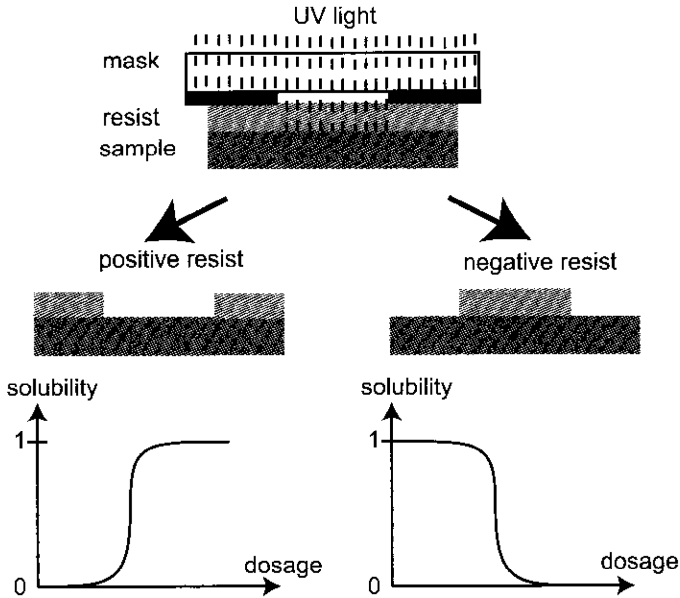

Figure 4.9: Top: contact illumination. The mask pattern is transferred into the resist via illumination and subsequent development. Center: resulting resist cross section for positive (left) and negative (right) resist. Bottom: Solubility characteristics for the two resist types.

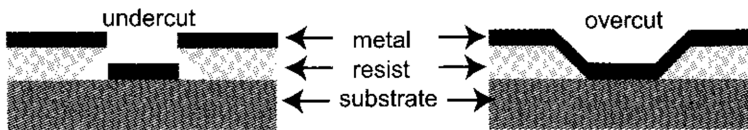

Figure 4.10: Overcut (left) and undercut (right) resist profile after illumination, development, and surface metallization.

that the smallest feature sizes are about half the wavelength ($\approx$ 150 nm), divided by the index of refraction of the resist ($\approx$ 1.5), which limits the resolution to roughly 100 nm. The mask can be a quartz plate coated with a thin chromium film, which contains the pattern to be illuminated. In the contact illumination scheme, the Cr film is in mechanical contact with the resist and blocks the light, such that the resist underneath the Cr remains unexposed.

During contact illumination, the mask suffers contaminations due to dust particles on top of the resist, as well as by resist adhesion. This can be avoided by projection illumination, where the mask pattern is transferred into the resist via lenses. This technique is widely

used in industry, but somewhat unusual in research labs.

The photoresists can be classified as *positive* and *negative*. The solubility of the exposed areas increases for a positive resist, while it decreases in negative resist, see Fig. 4.9. Immersing the sample into a suitable developer removes the corresponding sections of the resist film. Both types of resists have in common that their solubility as a function of the illumination dosage is a step-like function. This ensures high resolution and sharp edge profiles. It may seem irrelevant at first what kind of resist is used in a particular process. There may, however, be some process specific requirements which favor one type or the other. Most importantly, negative resist predominantly produces an *undercut profile*, which means that after development, the resist area in contact with the sample is smaller than the area at the resist surface, Fig. 4.10. This is a consequence of the approximately exponentially decreasing intensity of the illuminating light as it penetrates into the resist. An undercut profile is highly desirable for subsequent metallization steps, in which the resist itself serves as mask. After the metallization, the resist including the metal film on top usually has to be removed in a *lift-off* step , which is bound to fail for resists with an overcut profile, since the metal on the sample and that one on top of the resist are connected. An undercut profile avoids this problem, provided the thicknesses of metal layer and resist are properly selected. [2]

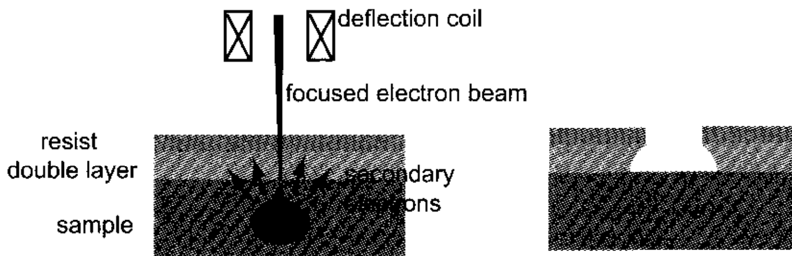

Figure 4.11: Left: a focused electron beam is scanned across the sample surface with a pattern generator that drives the deflection coils, which are part of the electron optics of the electron microscope. The electrons get scattered both elastically and inelastically in the substrate, and secondary electrons are generated, which have a large cross section for resist illumination. The resulting profile of a two-layer electron sensitive resist after illumination is shown to the right.

In principle, the resolution can be increased by using shorter wavelengths. In X-ray lithography, resists are illuminated with wavelengths in the 10 nm regime. While significant progress has been achieved over the past decade, severe technological obstacles have to be overcome before this version of optical lithography can be widely used. Photoelectrons limit the resolution to several 10 nm, and optical components as well as masks are difficult to fabricate, since metals get transparent in the UV. The ultimate limit of such lithographic techniques is set by the resolution of the resists, which contain organic

[2]It should be mentioned that techniques exist for achieving undercut profiles with positive resist as well.

polymers. The cross linking of the polymers is enhanced or reduced by the light, which modifies their solubility accordingly. Thus, the resolution cannot become better than the size of the corresponding monomers, which is of the order of 0.5 nm. For feature sizes

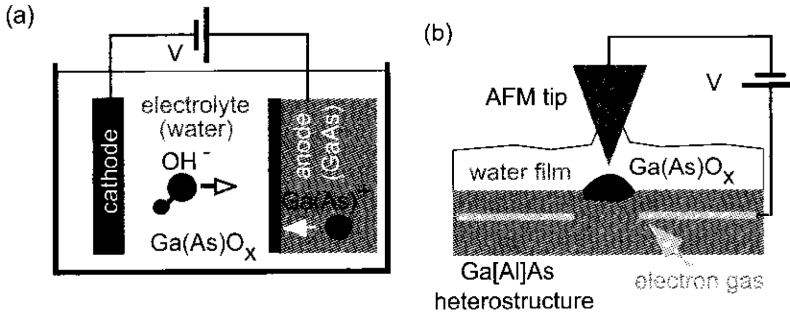

Figure 4.12: (a): scheme for conventional anodic oxidation of GaAs. (b): downscaled version of anodic oxidation, with the conductive tip of an atomic force microscope as the cathode, and the water film on top of the sample as electrolyte.

below $\approx$ 150 nm, electron beam lithography is the current technique of choice.

2. Electron beam lithography
   Instead of light, electrons may be used as well for illuminating resists, which are in this case polymers like PMMA (poly-methyl metacrylate) with a well-defined molecular weight. In a positive resist, the electron beam breaks the bonds between the monomers, and an increased solubility results. In negative resists, on the other hand, the electron beam generates inter-chain cross linking, which deceases the solubility. In that respect, electrons ave a very similar effect as UV light on the resist. A typical experimental setup is shown in Fig. 4.11. A focused electron beam is scanned in a predefined pattern across the sample using deflection coils in the electron optics. In contrast to optical lithography, this is a serial and therefore a slow process. However, structure sizes of 50 nm and even below can be fabricated. Many research groups use electron beam lithography in the lab for all feature sizes below 2 microns or so, because the technique gives very good and reproducible results. One type of electron beam lithography uses a high energy beam of electrons (about 30 keV or larger), which produces extremely small spot sizes of about 1 nm only. However, the illumination resolution is worse than this, since the spatial distribution of secondary electrons backscattered from the substrate actually illuminate the resist, Fig. 4.11. Since the intensity of those electrons drops from the substrate towards the surface of the resist, an undercut profile is intrinsic to this process. The undercut is often enhanced by a two- layer electron beam resist with different dosages.

Direct writing methods

Per definition, such methods do not require resists. Rather, the sample is patterned directly by the exposure. The number of process steps (see Fig. 4.8) is reduced from 5 or 6 to just one.

We briefly discuss two methods.

1. Focused ion beam writing
   The experimental setup resembles the electron writing system, with the electron source replaced by an ion source (e.g., gallium). The ions are implanted in the substrate and localize the electrons in the exposed areas. Highly resistive regions can be defined this way. However, the lateral depletion is rather large, typically above 100 nm. Suitable ion beams can also be used to dope the sample locally.

2. Scanning probe lithography
   As an example of current research activities, we briefly discuss lithography techniques based on scanning probe microscopes (SPMs) [Binnig1982]. Recently, tremendous progress has been made in this respect. Since SPMs achieve atomic resolution, they are highly promising tools for achieving a further, significant size reduction. Meanwhile, SPMs have been used in a wide variety of operational modes in order to modify surfaces [Marrian1993]. Moving single atoms with an SPM tip [Eigler1990], material deposition from the tip on the substrate [Mamin1990], has been demonstrated experimentally, for example. Amazing nanodevices can also be fabricated by scratching [Irmer1998]. Another widely investigated technique is local oxidation of the substrate. [Dagata1990] oxidized a variety of substrates locally by applying a negative voltage to the tip of an SPM with respect to the grounded substrate. Local oxidation with an atomic force microscope has also been used to pattern the electron gas in Ga[Al]As heterostructures directly [Held1998]. Anodic oxidation is a standard process to oxidize surfaces of metals and semiconductors. The setup for local oxidation with an AFM is essentially identical (Fig. 4.12). Here, the water film forming under ambient conditions on top of the substrate provides the electrolyte. A conductive AFM tip acts as cathode, while the chip to be nanostructured is grounded. As a result, the sample surface oxidizes in close vicinity to the AFM tip. The 2DEG is depleted underneath the oxide lines in shallow HEMT structures, provided the distance between 2DEG and sample surface is smaller than about 50 nm. The underlying mechanism can be understood in a simple picture: as the cap layer is oxidized, the semiconductor surface gets closer to the 2DEG, while the surface area, and thus the number of surface states, is slightly increased. In samples with the 2DEG so close to the surface, only $\approx 10\%$ of the donor electrons from the doping layer go into the 2DEG, while the remaining 90% fill the surface states. A small reduction of the distance between surface and the 2DEG changes the internal electric fields and can lead to depletion. We have seen several examples of Ga[Al]As-HEMTs patterned by this technique in the introduction.

Etching

An important technique of transferring the resist pattern into the sample is etching. Patterned resists can be used as etch masks, provided the etchant is sufficiently selective. We distinguish between dry etching and wet chemical etching.

1. Dry etching
   The setup for dry etching techniques consists of a vacuum chamber with two electrodes

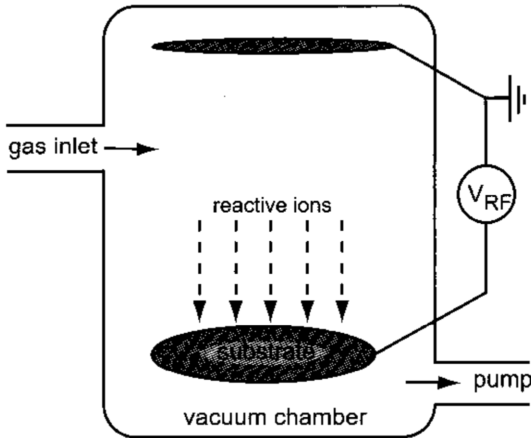

Figure 4.13: Scheme of a vacuum chamber for reactive ion etching.

at the top and the bottom. The sample is placed at the bottom, which may be the anode or the cathode, depending on the process. A gas discharge is ignited, and the ions of the etch gas hit the sample (Fig. 4.13). One speaks of plasma etching if the reaction is purely chemical. Oxygen plasma etching is often used to remove resist layers. The low energy ions avoid damage of the semiconductor and metal components of the sample. A purely physical technique, on the other hand, is ion etching. Here, suitably selected ions are generated and strongly accelerated towards the sample. The physical impact removes sample atoms. Here, resists may serve as masks for a limited time. Radiation damages in the sample, combined with the required high vacuum and the large rate of material deposition at the walls, make this a rather unusual technique. Widely used, however, is *reactive ion etching*. Here, both the physical and the chemical aspects of the ionic exposure are important. A very convenient side product in this kind of etching a polymer formation at the etched walls, which prevent lateral removal of material. As a consequence, very steep and deep grooves can be etched.

2. Wet chemical etching
   Wet chemical etching means immersing the sample in a suited etchant solution. In contrast to metals, the majority of the common semiconductors are not attacked by pure acids. Therefore, the etch typically consists of a mixture of an oxidizer, such as H_2O_2, an acid, like HCl, and water. H_2O_2 oxidizes the semiconductor, while the acid removes the freshly formed oxide. The oxidation and etch rates depend on the etch composition as well as on the crystal direction. The resulting edge profile can thus be tuned accurately. For many purposes, an overcut edge profile is desirable, since often, thin metal layers have to be deposited on the surface later on. A metal layer thinner than the etched depth may get disconnected across an etched step with undercut profile.

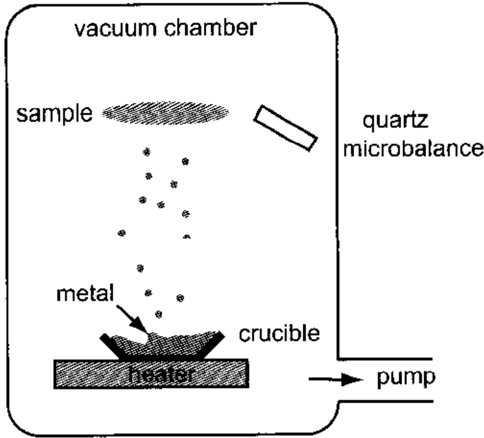

Figure 4.14: Scheme of an evaporation system for metallizations.

4.1.4 Metallization

By metallization, we mean the deposition of metal films on the semiconductor surface. This is usually done by evaporation of the metal in a vacuum chamber. The metals are molten (or sublimed, respectively) in a crucible made of tungsten of carbon, which can be done by heating the crucible with a current, or by focussing an electron beam onto the metal, see Fig. 4.14. At sufficiently large temperature, the metal vapor pressure is so high that a metal film grows at the exposed surfaces with a rate of the order of a nanometer per second. The film thickness is monitored by an oscillating quartz plate. As the metal gets deposited on the quartz, its resonance frequency gets smaller. This effect can be calibrated, and the film thickness can be measured with high accuracy. For lift-off processes, the film thickness should be smaller than the thickness of the resist, for obvious reasons. Typical metallization layers measure thicknesses between 20 nm and a few microns.

Of particular importance for the fabrication of nanostructures is the so-called *angle evaporation technique* [Dolan1977], because feature sizes below the lithographic resolution can be made this way. The trick is to evaporate successive layers of metals from different angles and use the resist as a shadow mask. The technique is illustrated in Fig. 4.15. Overlap areas as small 30 nm by 30 nm can be fabricated routinely by angle evaporation.

As pointed out in the previous chapter, metal-semiconductor interfaces form Schottky barriers for the vast majority of material combinations. In order to obtain an Ohmic contact, a suitable metal film is evaporated and afterwards alloyed into the semiconductor. "Suitable" means that the Schottky barrier should be small, the metal should have a low melting point and should act as a dopant in the semiconductor. For GaAs, the $\mathrm{Au}_{0.88}\mathrm{Ge}_{0.12}$[3] eutectic alloy is a standard Ohmic contact material. The Schottky barrier of the $\mathrm{Au}_{0.88}\mathrm{Ge}_{0.12} - \mathrm{GaAs}$ system is only 0.3 eV, In addition, eutectic AuGe has a melting point of 360 °C, and already at

[3]The numbers here mean the weight fraction.

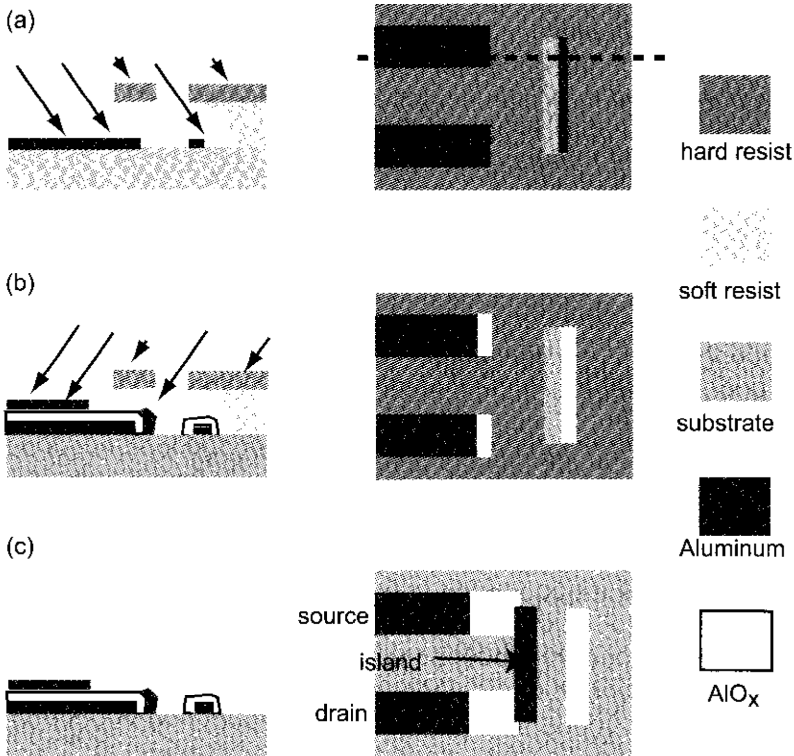

Figure 4.15: Angle evaporation. The right column shows a top view of a sample section after illumination by electron beam lithography, development, and subsequent evaporation of aluminum under a certain angle. To the left, a cross sections of the layers along the dashed line in the right figure is shown. A layer of electron beam resist with low dosage is covered by a resist with a higher dosage. This leads to cage formation as an extreme version of an undercut profile. The upper resist layer is free-standing over a certain area. In (b), the Al gets oxidized, and a second Al layer is evaporated on top at a different angle, as indicated by the arrows. A sandwich structure with small overlap areas results, which can be below the pattern sizes in the resist mask. In (c), the resulting structure, a small Al island coupled to two leads via small-area tunnel barriers, is shown after the resist layers have been removed. Such islands will be investigated further in chapter 9.

420 °C, it begins to alloy into GaAs. Ge atoms diffuse into the Ga and act as donors. This diffusion can be enhanced by adding a small fraction of Ni to the alloy. The resistivity of such a contact is of the order of 10^{-6} Ωm. The low process temperatures are important, since they ensure Ohmic contact formation well below critical temperatures for other processes, such as Si dopant migration in GaAs, which would damage the modulation doping profile.

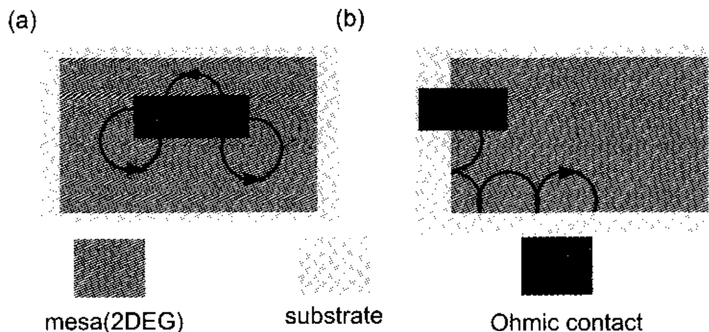

Figure 4.16: In strong magnetic fields, electrons move in cyclotron orbits and thus remain localized close to the Ohmic contact (a), unless the contact crosses the mesa edge (b).

Finally, one small technical note should be made here. Since in many cases, mesoscopic transport experiments involve application of strong magnetic fields, it is very important that the Ohmic contacts extend across the mesa edge. Otherwise, the contact resistance increases sharply in strong magnetic fields, since the electrons move in cyclotron orbits in the electron gas, and localize within a small area around the contact, see Fig. 4.16. This problem arises in particular in two-dimensional electron gases and at cyclotron radii below the mean free path.