A new FDSOI spin qubit platform with 40nm effective control pitch

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presented by Simon Geyer

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Contents

• state-of-the-art
• simulations
• fabrication
• RT characterization
• low-T characterization
State-of-the-art FDSOI platform

- 300mm process with immersion-DUV litho
- linear chain of electron/hole qubits
- 2xN arrays of QDs (face-to-face gates)
- natural barriers by self-aligned spacers
- global top- and back-gate
- high-temperature single-shot spin readout (PSB)
- single-shot qubit readout (Elzerman)

Hutin et al., IWDM 2019
Duan et al., Nano Lett. 2020
State-of-the-art FDSOI platform

• problem: no control over tunnel barriers if each gate accumulates one QD
State-of-the-art FDSOI platform

• problem: large QDs needed for scheme with QD below every second gate -> no quibts

Vivien Schmitt, APS march meeting 2022
New FDSOI platform

• Solution: local exchange gates (J-gates)
Simulations

- Poisson + effective mass simulation
- Periodic structure of 2xN array
- Two modes:
  - Face-to-face coupling (readout)
  - Longitudinal coupling (2-qubit gates)
Simulations

• Poisson + effective mass simulation
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\[ D = \text{first gate layer thickness} \]

\( t = \begin{array}{c|c|c}
V_{bg} = 0 \text{ V} & V_{bg} = -2 \text{ V} & V_{bg} = -4 \text{ V} \\
10^3 & 10^1 & 10^1 \\
10^1 & 10^{-1} & 10^{-1} \\
10^{-1} & 10^{-3} & 10^{-3} \\
10^{-3} & 10^{-5} & 10^{-5} \\
10^{-5} & 10^{-7} & 10^{-7} \\
\end{array} \]

\[ t_{\parallel} \quad t_{\perp} \]

\( V_j (\text{V}) \)

\[ \begin{array}{c|c|c|c|c}
D = 50 \text{ nm} & D = 40 \text{ nm} & D = 30 \text{ nm} & D = 20 \text{ nm} \\
10^0 & 10^{-2} & 10^{-4} & 10^{-6} \\
10^{-2} & 10^{-4} & 10^{-6} & 10^{-8} \\
10^{-4} & 10^{-6} & 10^{-8} & 10^{-10} \\
10^{-6} & 10^{-8} & 10^{-10} & 10^{-12} \\
\end{array} \]

→ simulation shows more control than with global top gate

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Fabrication

- 300mm wafer scale using 193nm immersion DUV
- mesa: ~20nm Si, BOx: 145nm
- gate stack:
  - 2.5nm SiO$_2$ + high-k?
  - ~7nm TiN / 25nm polySi
- gate pitch: 80nm
- spacer: 25(?)nm SiN
- contacts
  - epitaxial growth: Si:P or SiGe:B
  - NiPt silicidation
- E-beam litho: trenches for J-gates (material?)
- effective pitch: 40nm
RT characterization

• from now on: only 1D arrays of electron QDs
• mass test of 2500 DQD devices (2 plunger+ 3 J-gates)
• 98.3% yield in leakage test of J1
• 90nm pitch devices
• select 79 out of 384 4-QD devices that work nicely (4 plunger + 5 J-gates)
• \( \rightarrow \) yield 21%
• test variability in G1-G4 (old gate layer)
• test variability in J (new gate layer)
• all J-gates shorted
• gate pitch 80, 90 and 100nm

TCAD:
Low-T characterization: QD

- back to DQD devices (2 plunger+ 3 J-gates) at 4.2 K
- back gate +25V to push QD to back interface
- operate as single QD
Low-T characterization: DQD

• tune from single QD to DQD using J-gate voltage
Role of gates

- Is switching the role of P and J-gates beneficial?

<table>
<thead>
<tr>
<th>2nd metal level:</th>
<th>1st metal level:</th>
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</thead>
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<tr>
<td>$E_C$</td>
<td>$E_C$</td>
</tr>
<tr>
<td>4.04meV</td>
<td>3.93meV</td>
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<td>$\alpha$-factor</td>
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<tr>
<td>0.025</td>
<td>0.30</td>
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<tr>
<td>$C_G$</td>
<td>$C_G$</td>
</tr>
<tr>
<td>$9.88 \times 10^{-19}$F</td>
<td>$1.24 \times 10^{-17}$F</td>
</tr>
</tbody>
</table>

Bruna Paz, APS March Meeting 2022
Conclusion

- new device layout with 40nm pitch
- simulations predict subthreshold slope and tunneling rates
- RT characterization shows good yield for DQD devices and small variability for pre-selected sample of 4QD devices
- 4K characterization shows control over tunnel coupling of neighboring QDs
- quantitative study of tunneling rates vs $V_J$ is to be shown

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