QUBUS AND PARITY CHECKS

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Weight-four parity checks

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Weight-four parity checks with silicon spin qubits

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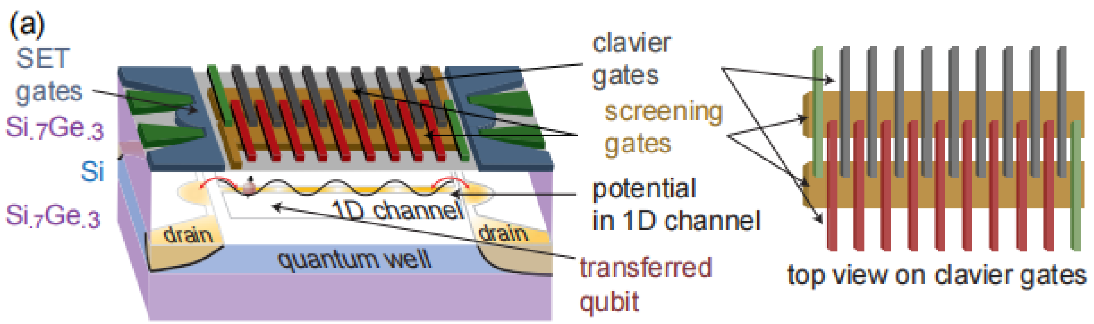
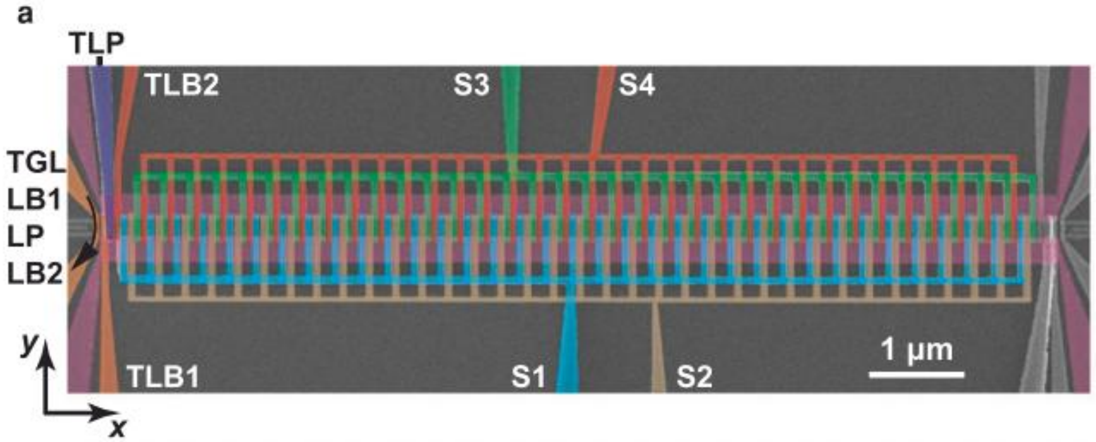
Recent advances in coherent spin shuttling have made sparse semiconductor spin qubit arrays an appealing solid-state platform to realize quantum processors. The dynamic and long-range connectivity enabled by shuttling is also essential for many quantum error-correction (QEC) schemes. Here, we demonstrate a silicon spin-qubit device that comprises a shuttling bus for coherently transporting qubits that can interact at four isolated locations we call bus stops. We dynamically populate the array and tune all single- and two-qubit operations using shuttling and quantum non-demolition (QND) spin measurements, without access to charge sensing in most of the device. We achieve universal control of the effective five-qubit processor and select the connectivity required to form a surface-code stabilizer plaquette that supports X- and Z-type parity checks up to weight-four. We use the parity checks to generate multi-qubit entanglement between all qubit combinations in the array and report the genuine entanglement of a five-qubit Greenberger-Horne-Zeilinger (GHZ) state, constituting the largest such state ever constructed with gate-defined semiconductor spins. This work opens immediate opportunities to pursue QEC experiments with spin qubits, and the protocols developed here lay the groundwork for the modular calibration and operation of sparse spin qubit arrays.

- Bus + bus-stop design, achieve the Quantum non-demolition (QND) parity readout
- Weight-2 to weight-4 parity measurement
- 2-5 qubit GHZ state

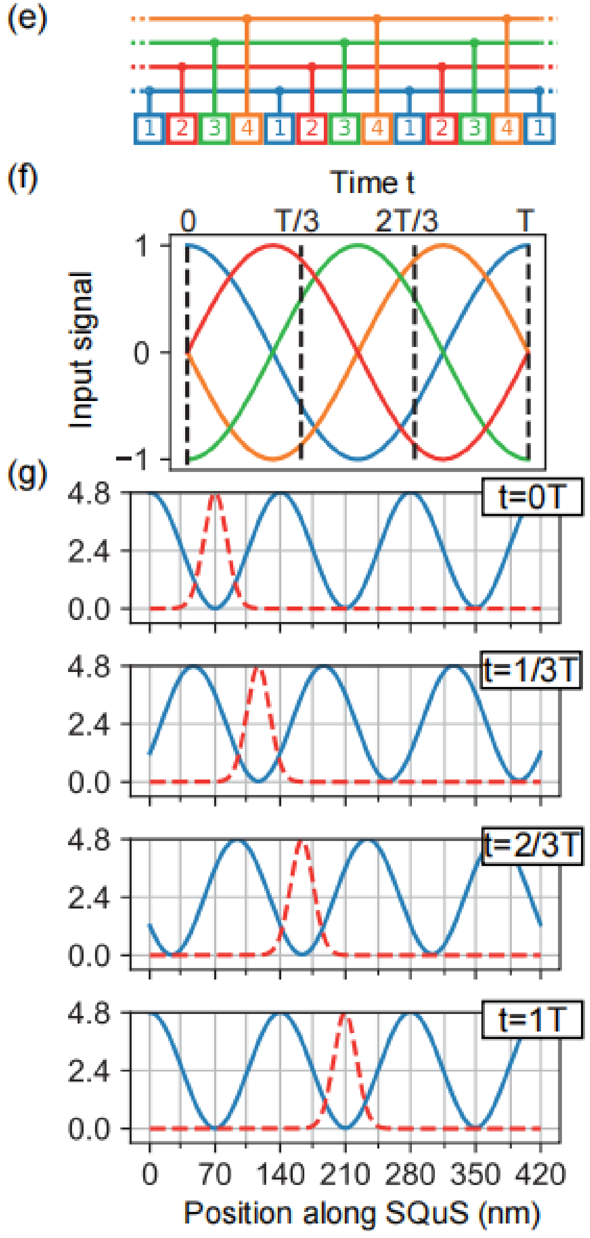
Conveyor-Belt Mode





Spin shuttles using a moving potential wave:

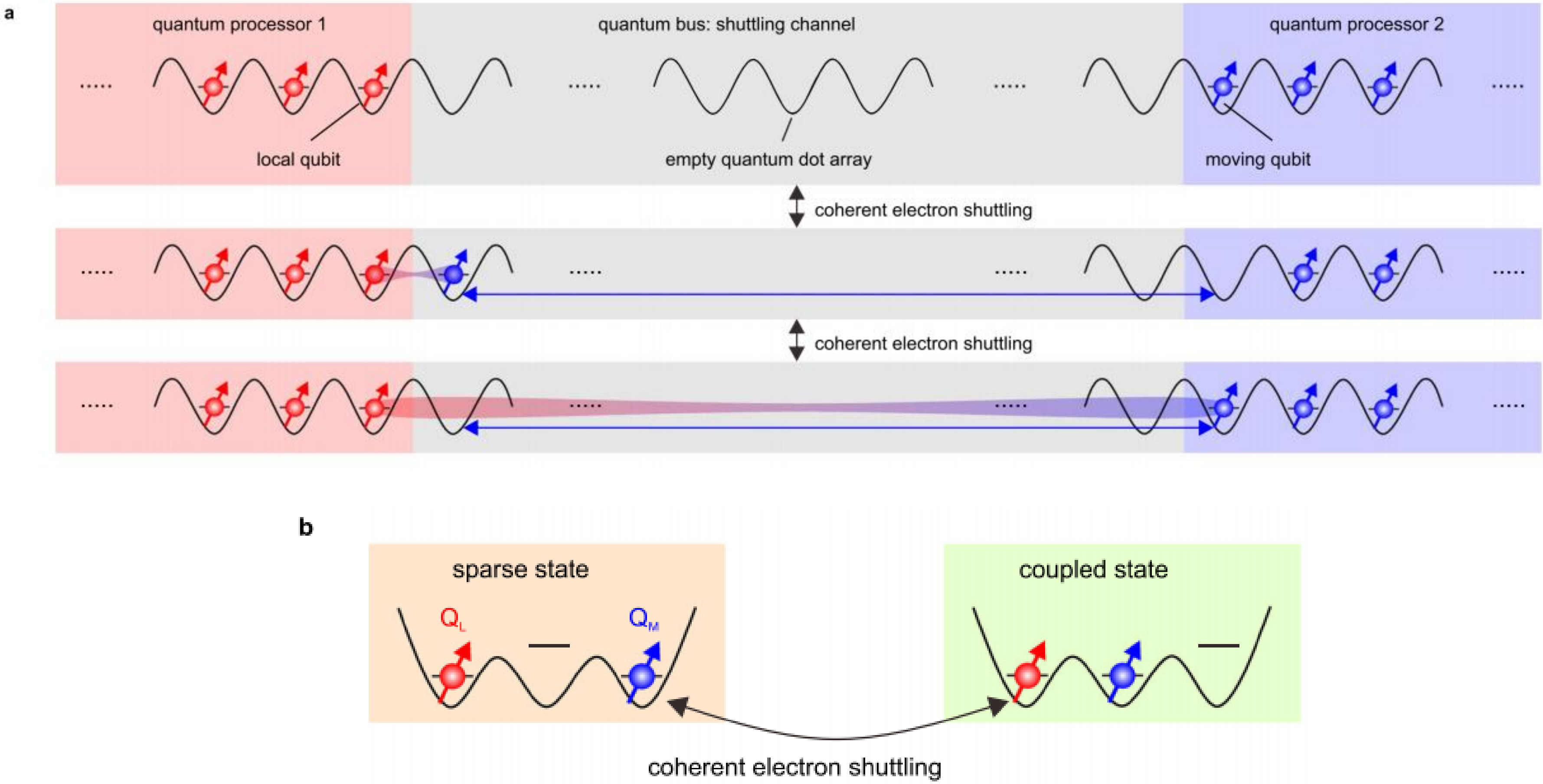
- A series of electrostatic gates generate a traveling wave potential that traps and transports electrons sequentially.
- The wave moves at a controlled speed, ensuring electrons are shuttled without losing their quantum state



$$V_{si}(\tau_S) = U_i \cdot \sin(2\pi f \tau_S + \phi_i) + C_i$$

Langrock et al., PRX Quantum 4, 020305 (2023)
Xue et al., Nat. Commun 15, 2296 (2024)

Exchange Gate from Shuttling

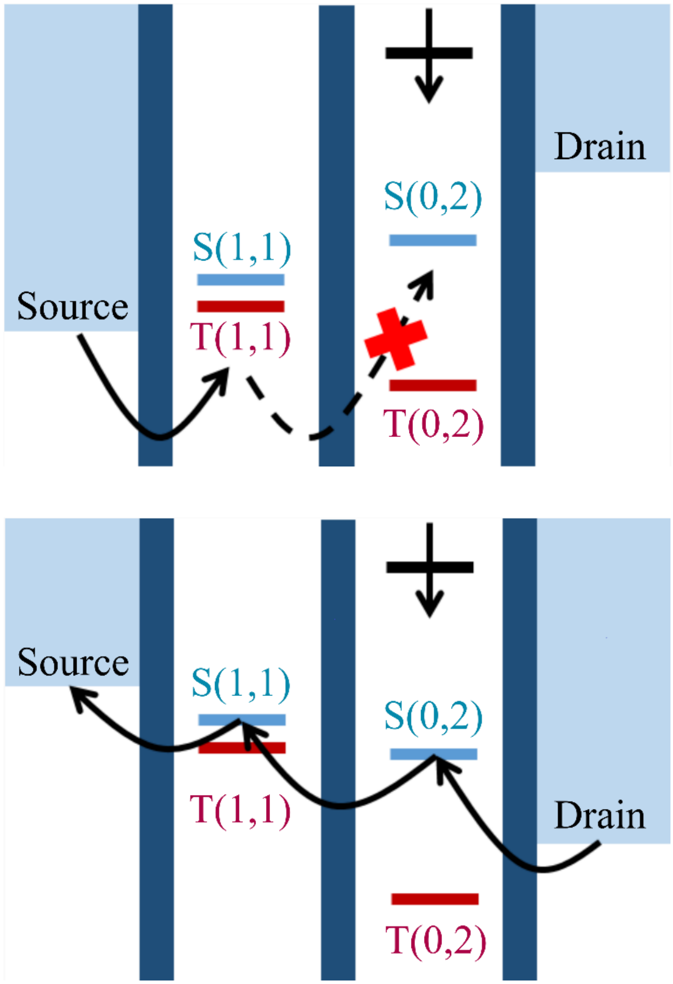


Shuttling the spin to control the exchange coupling between 2 qubits → kill the residual exchange more efficiently

Akito Noiri et al., Nat. Commun., 13, 5740(2022)

Parity Check & PSB

PSB



Parity Check

State	Result
00	1
11	1
01	-1
10	-1

- Advantage of parity check:

1. Direct measurement of two-qubit correlations
2. Potentially quantum non-demolition (QND)
3. Compatible with quantum error correction: surface code

Device Layout

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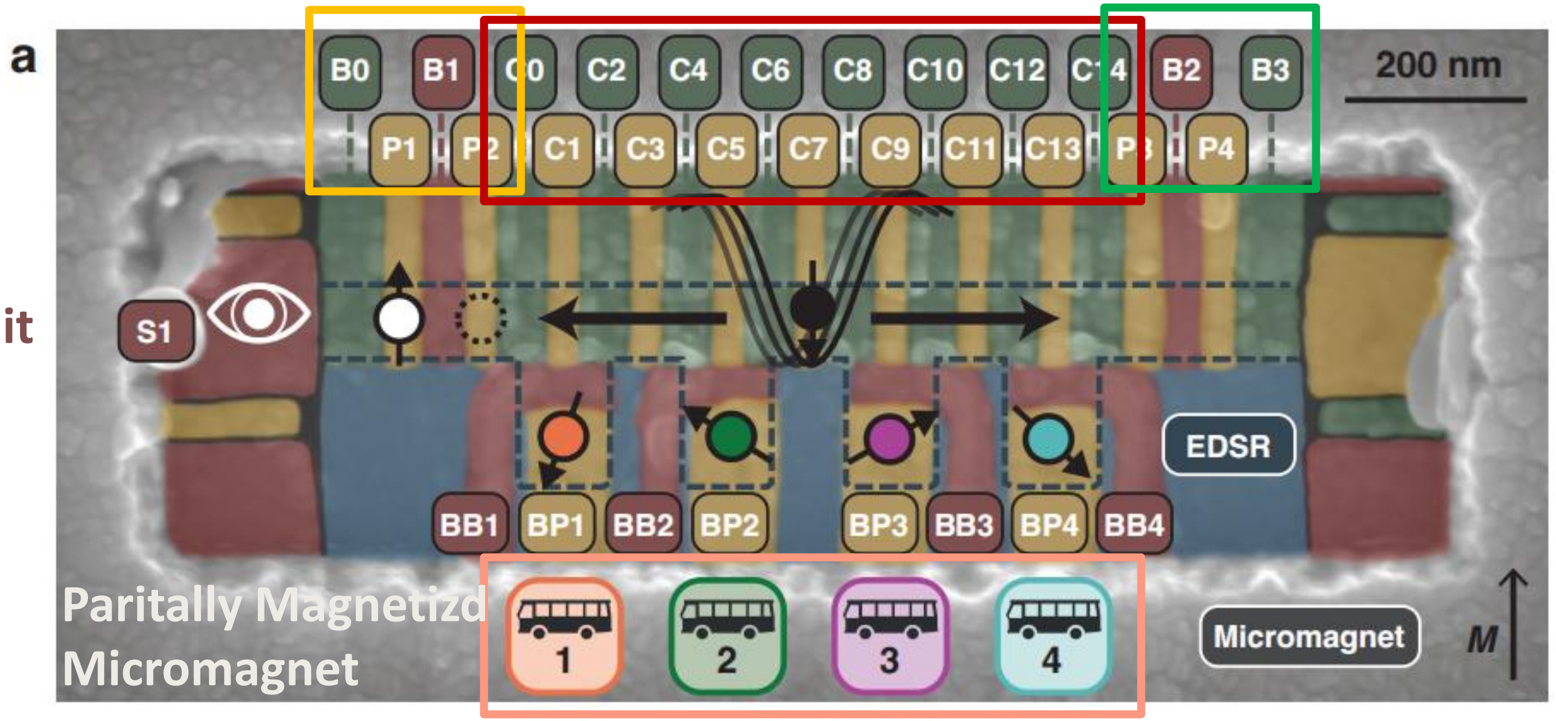
Purified Si/SiGe

Readout Zone

Shuttling Bus

Readout Zone (unused)

SET, Tank Circuit



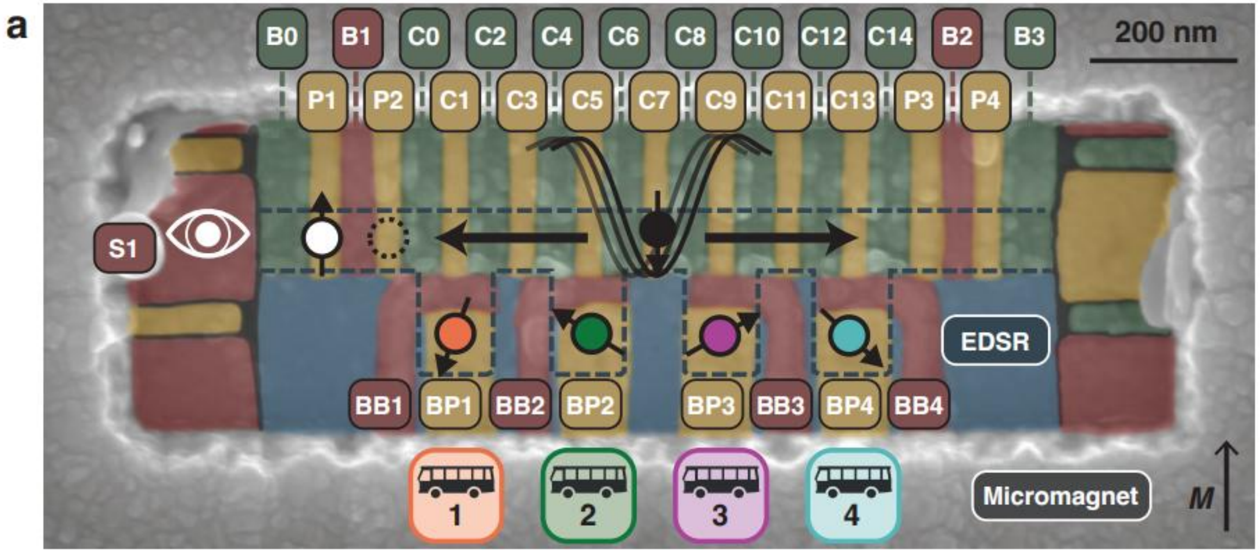
4 Bus Stops

Direct charge sensing ×
Shuttle the spin to readout zone √

Readout ancilla R1: constant under P1
Mobile ancilla A1: initial under P2

1. Load a mixing state spin in P2, wait 10 μs for initialization
2. Shuttle in the shuttling bus
3. Coupled with qubit in the bus stop
4. Shuttle back to P2
5. Parity readout

Shuttling Bus



- A1 can direct interact with D1-D4, R1 is used for parity readout to form a stabilizer
- Larmor frequency profile along the shuttling bus axis

Parabolic dependence: nonlinear dot displacement in a magnetic field gradient:

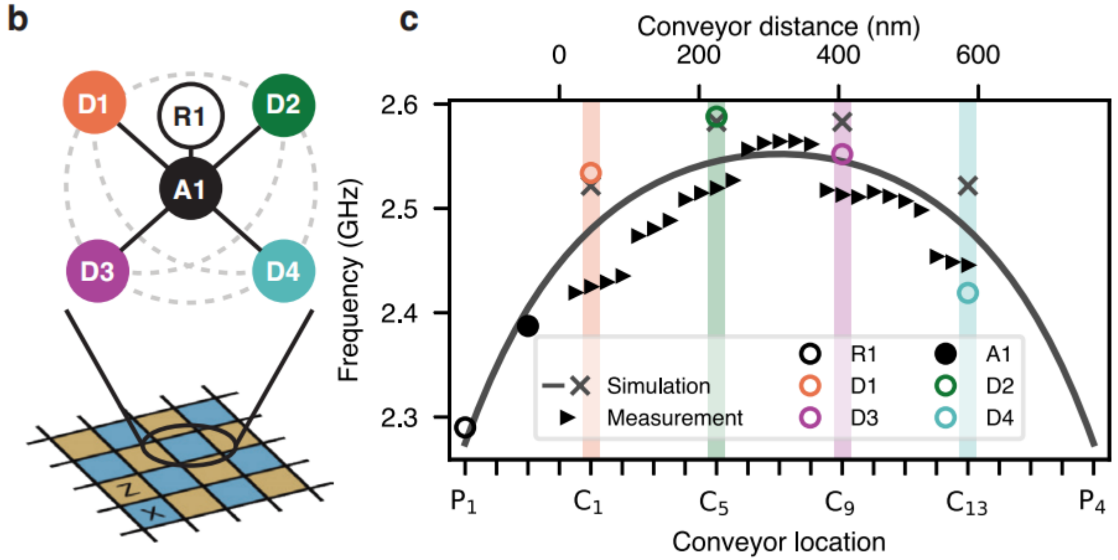
$$B_{\text{tot}} = B_0 + B_{\text{micro}}(x)$$

$$f_L = \hbar g \mu_B B_{tot} \propto B_{\text{micro}}(x)$$

Near the central of device the first order of magnetic field is small

$$B_{micro}(x) \approx B_0 x + B_2 x^2$$

Larmor frequency $f_L(x) \propto f_0 + \alpha x^2$



Remote Tuning

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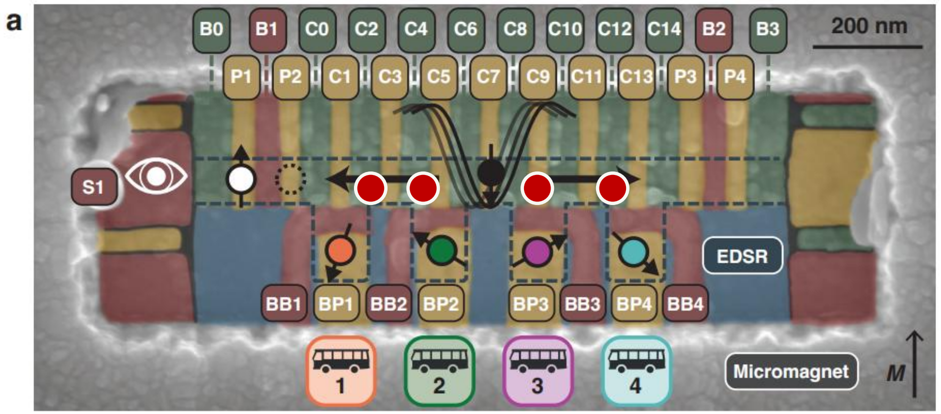
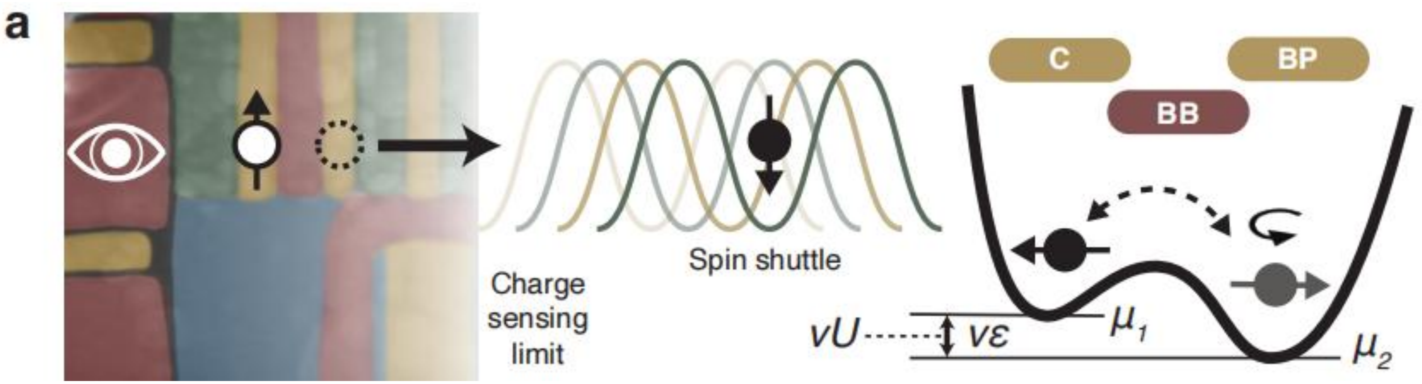
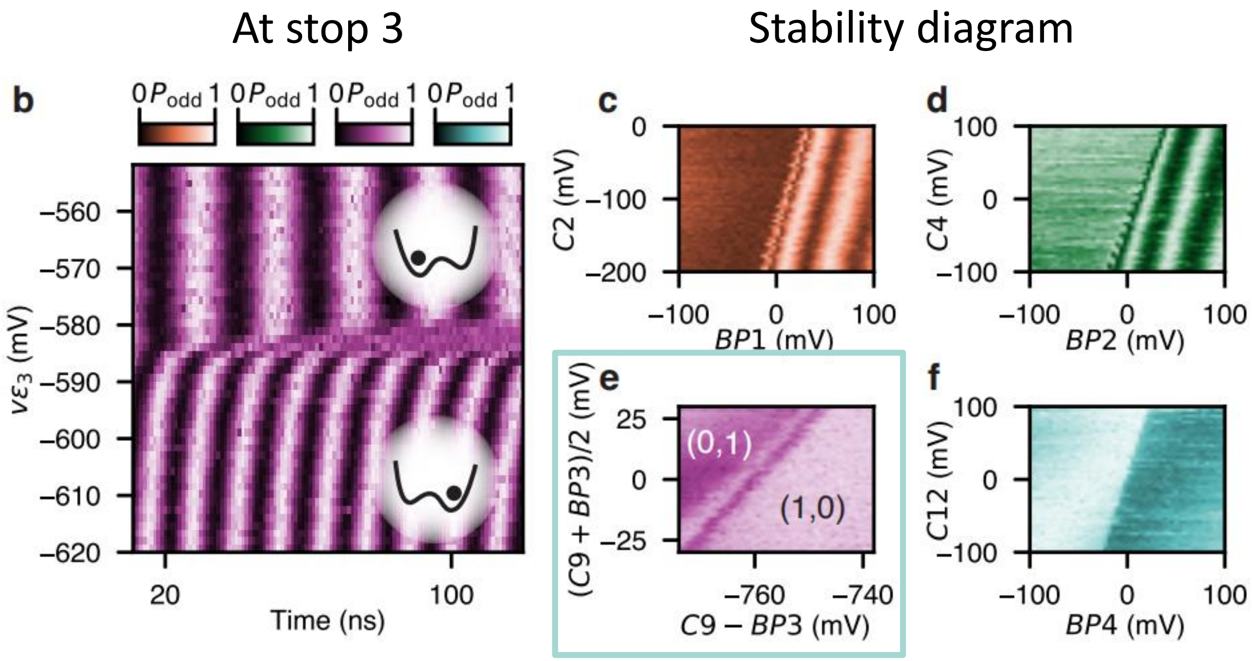


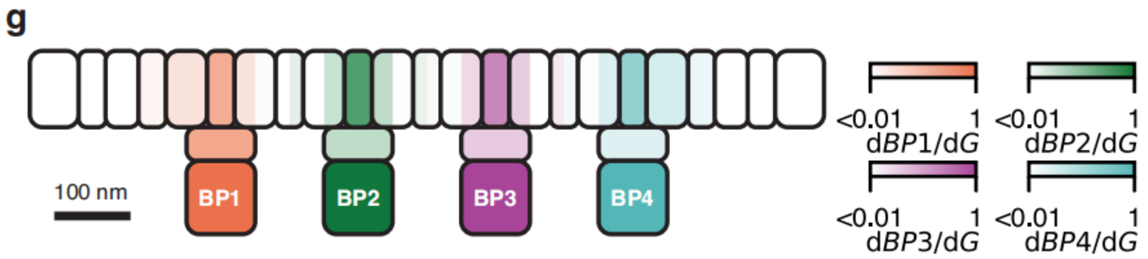


- A spin is placed in a superposition and shuttled to a bus stop out of charge sensing range
- Virtual detuning $v\epsilon \propto \mu_1 - \mu_2$
- Virtual chemical potential $vU \propto \frac{\mu_1+\mu_2}{2}$



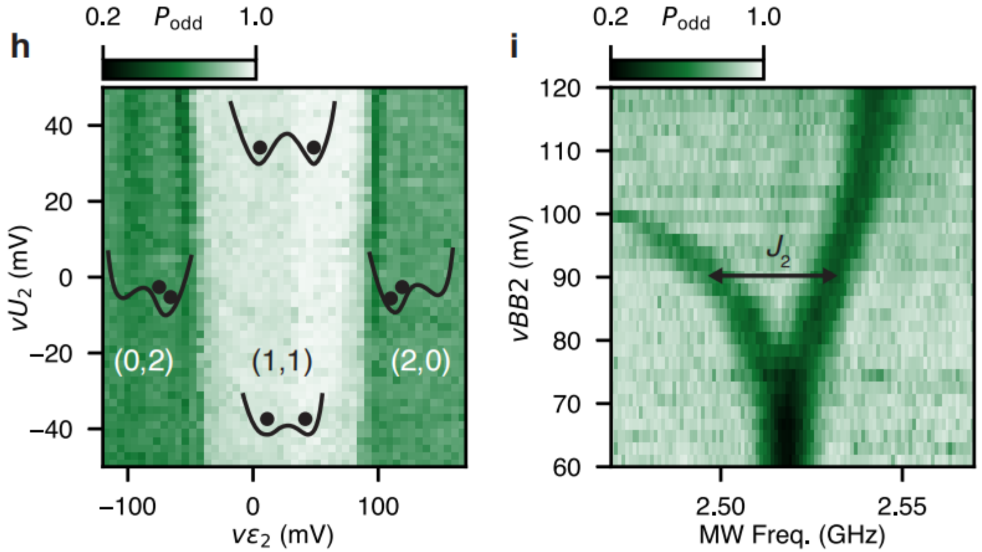
- Abrupt change in Larmor precession frequency shows the coherent tunneling of the ancilla spin
- Interdot transition between A1-Di to get the virtual gate
- Virtual gate: the relative capacitive coupling between all gates and the bus stop quantum dot
- Virtual detuning and virtual chemical potential control of the gate

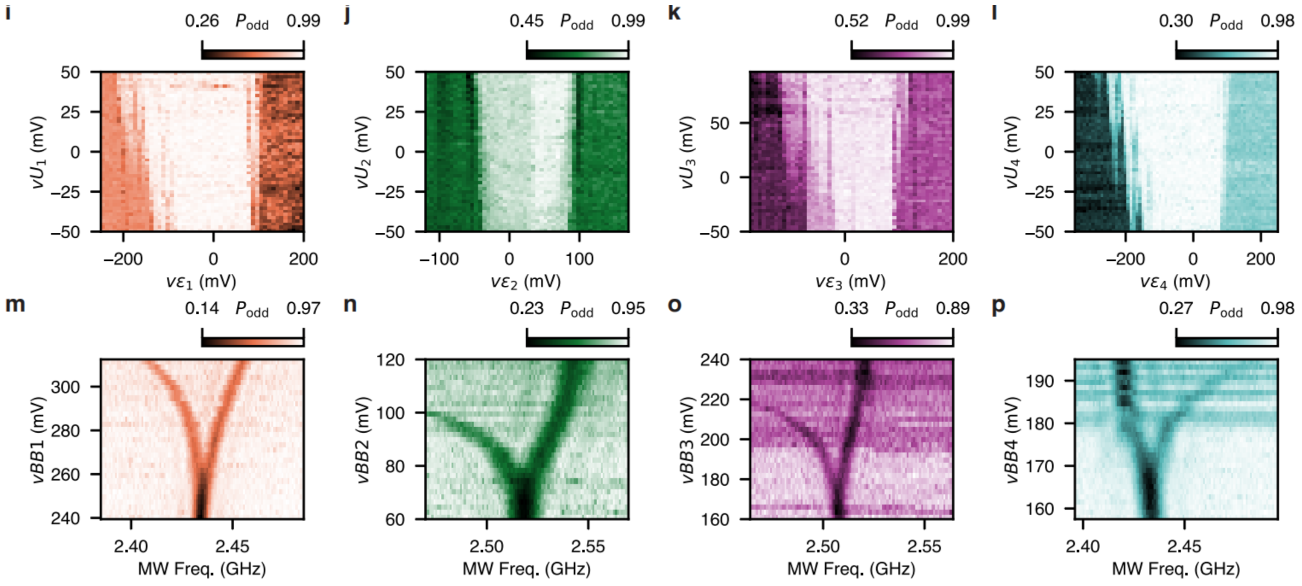
Virtual Gate



- Heatmap of all such electrostatic crosstalk
- Increase dot separation to ~200 nm to reduce crosstalk

At stop 2





- Virtualized charge stability diagram, identified from the returned polarization of a shuttled spin
- At the charge symmetry point, measure how exchange energy changes with virtual middle barrier→ tunability > 10 MHz, good for CROT and CZ

QND + Parity Check

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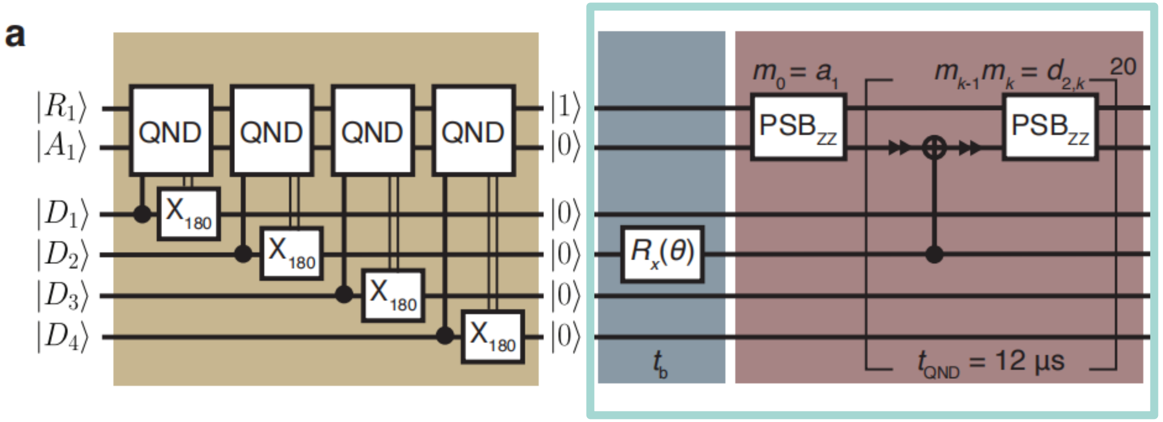
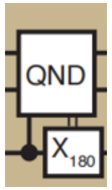
QND measurement circuit



- Shuttle A1 adjacent to Di, use CROT gate to flip A1 when Di is $|1\rangle$

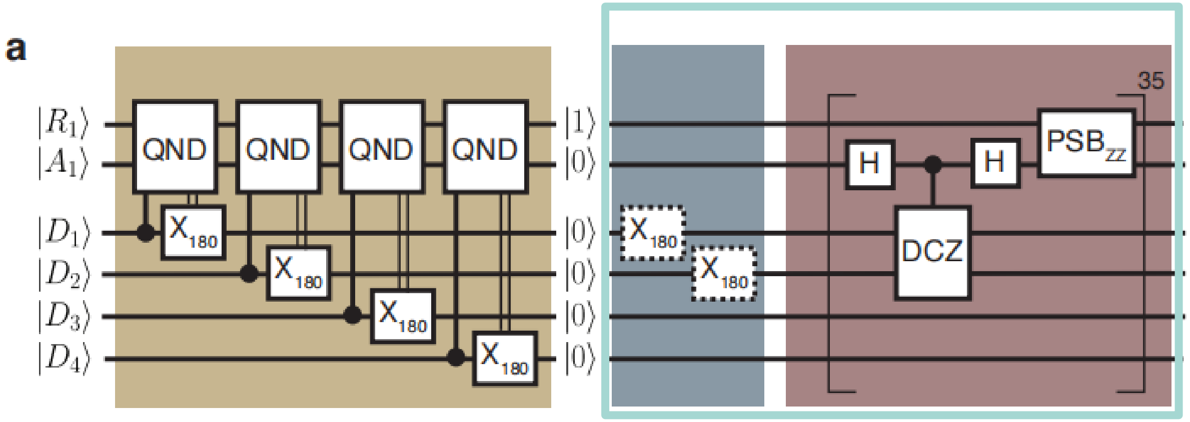


- Post selection: if we found the data qubit is flipped, X gate is applied to flip the qubit

$$CZ = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \end{pmatrix}$$

Parity Check Circuit

$$H\frac{|0\rangle+|1\rangle}{\sqrt{2}} = |0\rangle$$
$$H\frac{|0\rangle-|1\rangle}{\sqrt{2}} = |1\rangle$$



- QND readout: only measure ancilla, not the data qubit

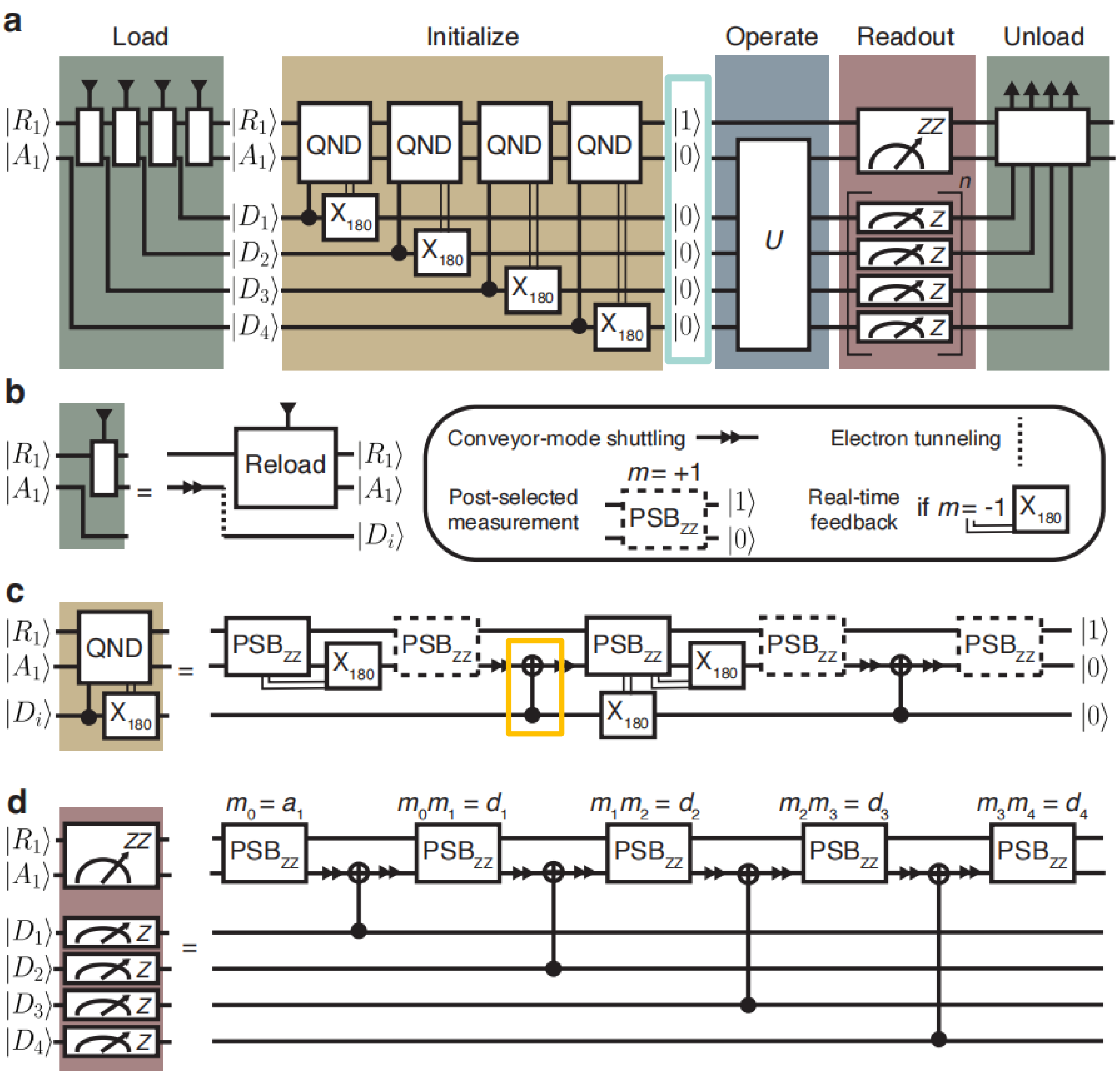
A1 $|0\rangle$ → (Hadamard gate) → A1 $\frac{|0\rangle+|1\rangle}{\sqrt{2}}$ → A1D1 $\frac{|00\rangle+|10\rangle}{\sqrt{2}}$; A1D1 $\frac{|01\rangle+|11\rangle}{\sqrt{2}}$

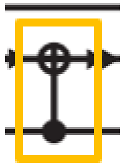
DCZ → A1D1 $\frac{|00\rangle+|10\rangle}{\sqrt{2}}$ → A1 $|0\rangle$

Hadamard gate

DCZ → A1D1 $\frac{|01\rangle-|11\rangle}{\sqrt{2}}$ → A1 $|1\rangle$

QND Measurement Framework





- CROT gate between A1-Di:

Di = 0, no change

Di = 1, flip the ancilla qubit A1

$$CROT(\pi) = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -1 \\ 0 & 0 & 1 & 0 \end{pmatrix}$$

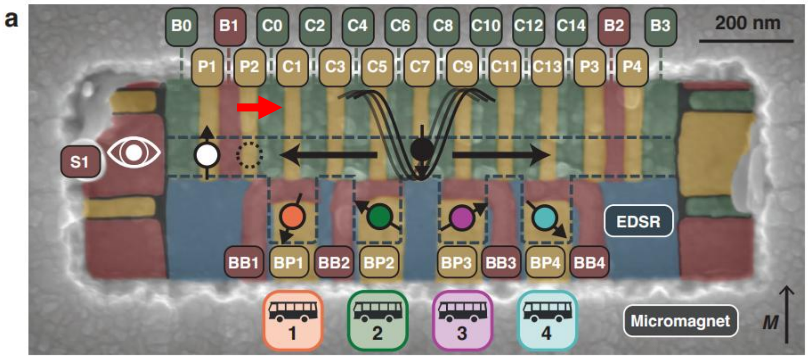
$$|10\rangle \rightarrow |11\rangle$$
$$|11\rangle \rightarrow -|10\rangle$$

- All four data qubits are loaded into bus stop in mixed state by shuttling ancilla qubit

- Load the ancilla qubit again from S1, initial both the ancilla and data qubits by measurement and using real-time feedback → higher fidelity

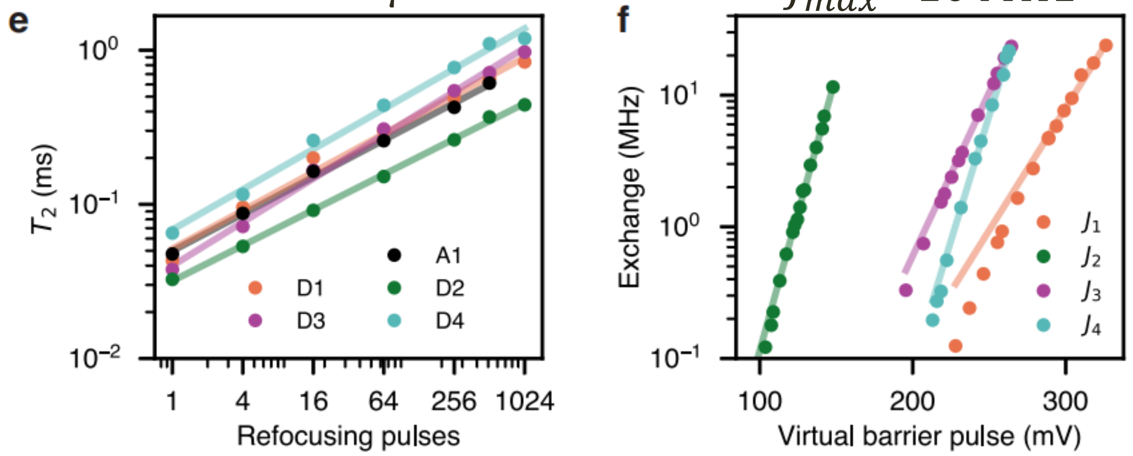
- The spin state of A1 changes with corresponding Di
- After measurement, the convey voltages return to 0 for unloading

Qubit characterization



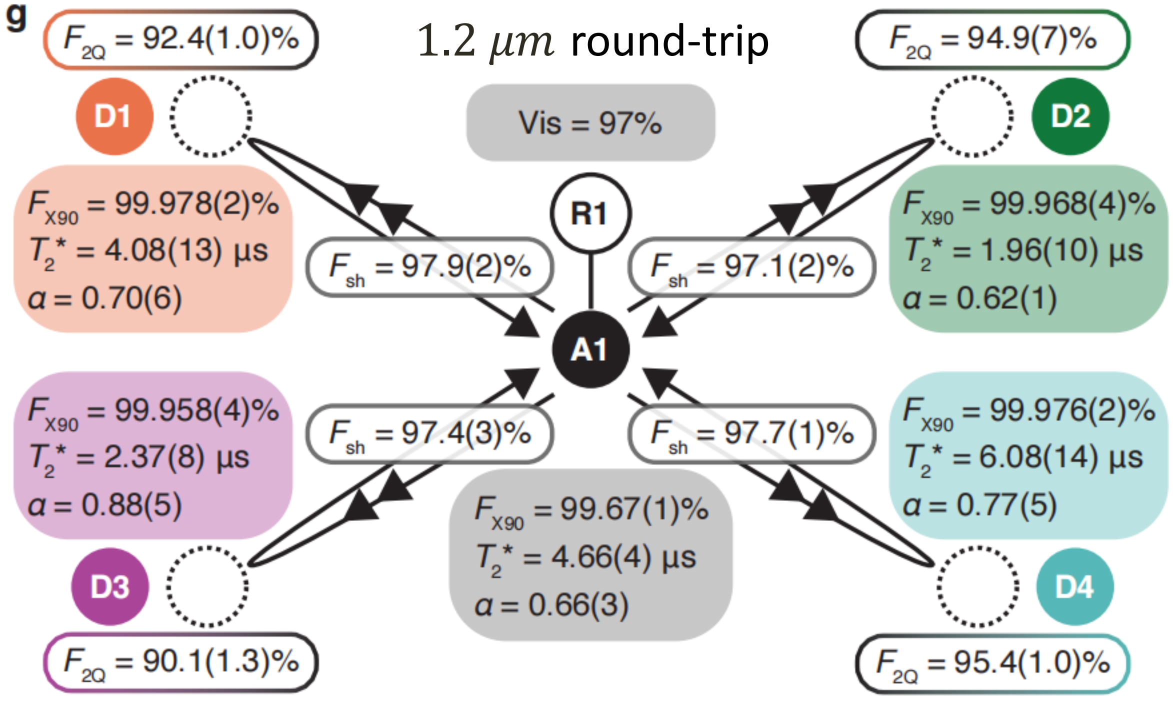
$\sim 10^2\ \mu s$

$J_{min} < 10\ kHz$
$J_{max} \sim 10\ MHz$



- CPMG coherence time. Main noise source: $\frac{1}{f^{\alpha}}$
- Readout 10 μs, whole experimental cycle ~300 μs
- Exchange tunability of all four interactions between data qubits and the ancilla

$1.2\ \mu m$ round-trip



F_{DCZ} (%)
84.2(8)
87.9(6)
82.8(1.3)
89.3(5)

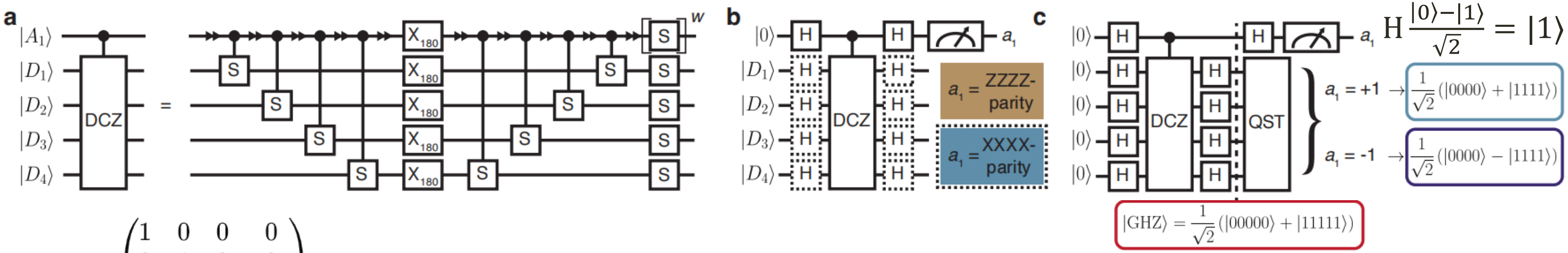
- Single qubit gate: high fidelity > 99.9%
- 2 qubit gate: 90%-95%. incoherence noise in the J, dephasing, valley excitation
- Shuttling:1.2 μm round-trip the longest coherent spin shuttle over a real distance in silicon

Benchmarking parity checks

Hadamard gate: $HXH = Z$

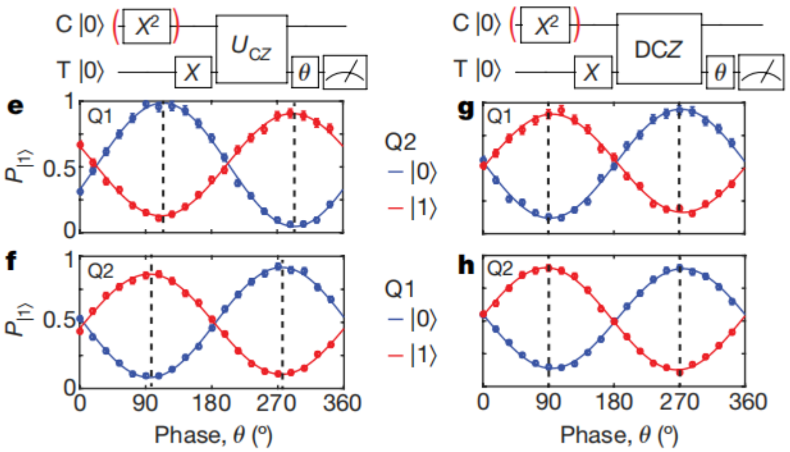
$$H\frac{|0\rangle+|1\rangle}{\sqrt{2}} = |0\rangle$$

$$H\frac{|0\rangle-|1\rangle}{\sqrt{2}} = |1\rangle$$



$$CZ = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \end{pmatrix}$$

- DCZ gate: ½ CZ gate + X gate + ½ CZ gate



$F_{DCZ} \sim 90\%$

A1 $|0\rangle$ —Hadamard gate→ A1 $\frac{|0\rangle+|1\rangle}{\sqrt{2}}$ —DCZ A1D1→ A1D1 $\frac{|00\rangle+|11\rangle}{\sqrt{2}}$

—DCZ A1D2→ A1D1D2 $\frac{|000\rangle+|111\rangle}{\sqrt{2}}$ —…→ GHZ $\frac{|00000\rangle+|11111\rangle}{\sqrt{2}}$

Watson et al., Nature 555, 633–637 (2018)

Benchmarking parity checks

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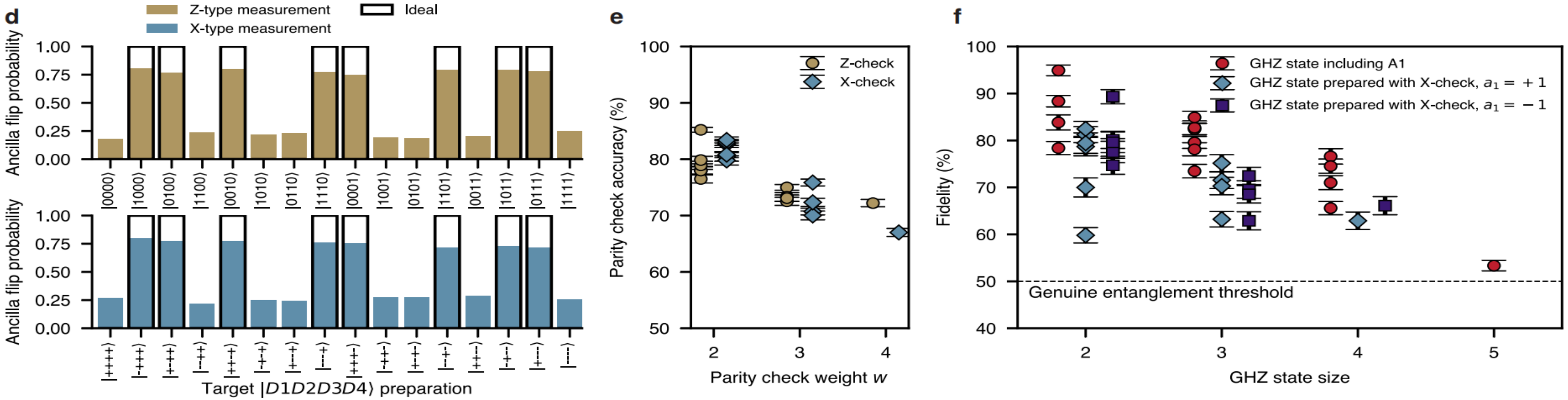
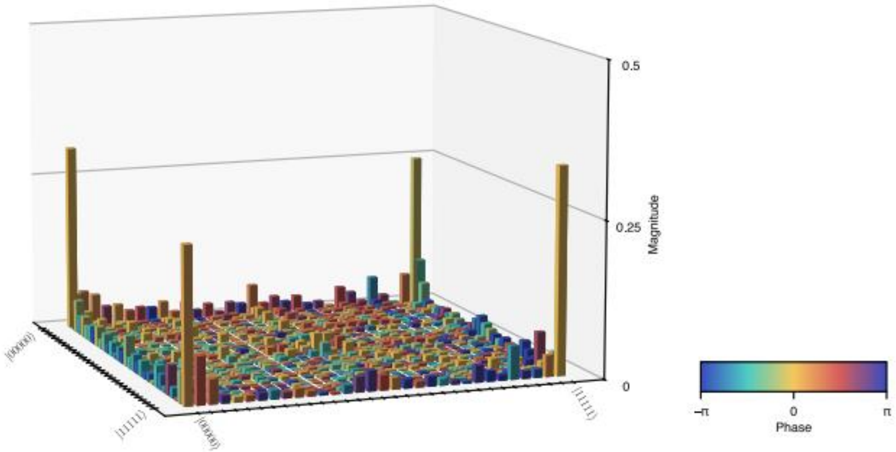


$$F_{parity} = \frac{P(even|even) + P(odd|odd)}{2}$$

GHZ $\frac{|00000\rangle + |11111\rangle}{\sqrt{2}}$

$F = 53.3(1.1)\%$
$F_{raw} = 32.6(0.4)\%$
A1 D1 D2 D3 D4



- Measured ancilla state when weight-four Z- and X-type parity checks: $F_{zzzz} = 72.2(6)\%, F_{XXXX} = 67.0(7)\%$
- The average probability A1 is correct and Di are measured in the intended prepared state
- Weight ω parity check accuracy is around 75%
- Weigh ω GHZ state Fidelity:
  - Weight 2 $F = 59.8\% \sim 94.9\%$
  - Weight 3 $F = 62.9\% \sim 84.9\%$
  - Weight 4 $F = 62.9\% \sim 76.6\%$
  - Weight 5 $F = 53.3(1.1)\%$

- Error:

1. Infidelity in the two-qubit exchange interactions.
2. Dephasing during shuttling and idling~25%

Conclusion and Outlook

Conclusion:

- Bus + bus-stop design, achieve the Quantum non-demolition (QND) parity readout
- Weight-2 to weight-4 parity measurement
- 2-5 qubit GHZ state

Next step for me to learn:

- Gate calibration
- Noise source and how to increase the fidelity