

Spin journal club: 3 July 2026



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Industry-compatible silicon spin-qubit unit cells exceeding ...

by P Steinacker · 2025 · Cited by 83 — **Industry-compatible silicon spin-qubit unit cells exceeding 99% fidelity** · Discussion. Device A exemplifies the high performance of qubits on ... [Read more](#)



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Harshit Choubey

Challenges on industrial-scale fabrication

charge noise reduction

static disorder arising from defects and traps at interfaces and oxides

High-fidelity single-qubit operations can be performed with minimal impact from charge noise

Other operations, including qubit initialisation, readout and exchange-based two-qubit gates are more sensitive to the charge noise present in conventional metal-oxide-semiconductor gate stacks

What makes this work important

Academic qubits

- High fidelity operations > 99%
- Low Scalability
- Prone to human variations

Industry

- Mass production at low costs
- Advanced fabrication process
- Uniformity

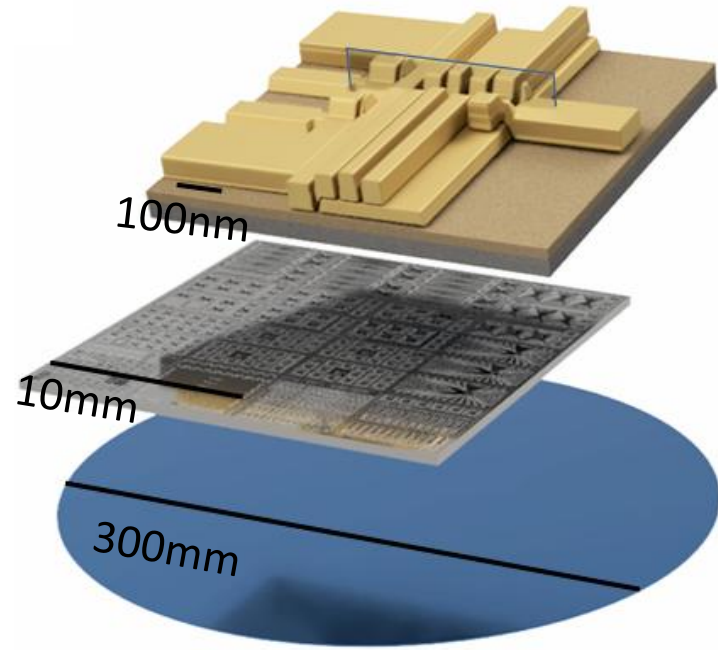
This work

Study four two-qubit devices fabricated using a long-established CMOS geometry with polysilicon gates on 300mm wafer scale.

Performed basic qubit operations, including one- and two-qubit gates, initialisation and readout, with low error rates.

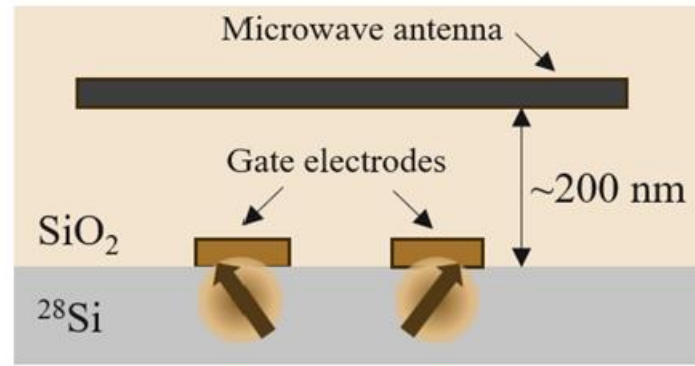
Error rates obtained using state-of-the-art gate set tomography(GST) allows pinpoint effects such as crosstalk and the breakdown between stochastic and coherent errors.

Device layout

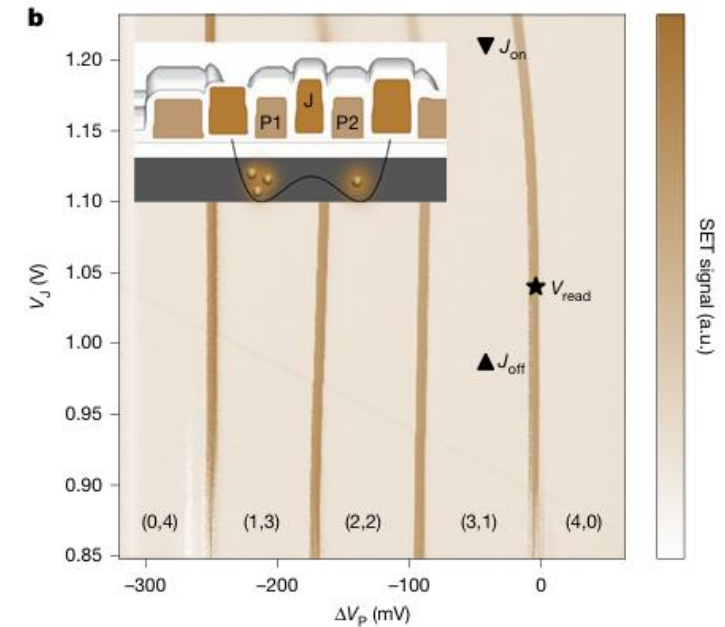


Si-MOS device

- Double quantum dot formed on Si –SiO₂ interface
- Single-electron transistor (SET) for spin read-out
- electrons were loaded from a 2DEG formed under the reservoir gate, which overlaps with an n++ implanted ohmic region
- Operated device in isolated mode, with four electrons in the double dot formed under P1 and P2.

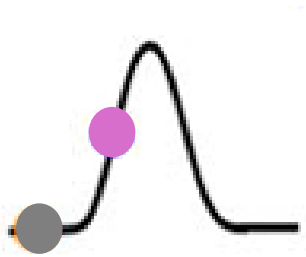


Mw antenna for ESR

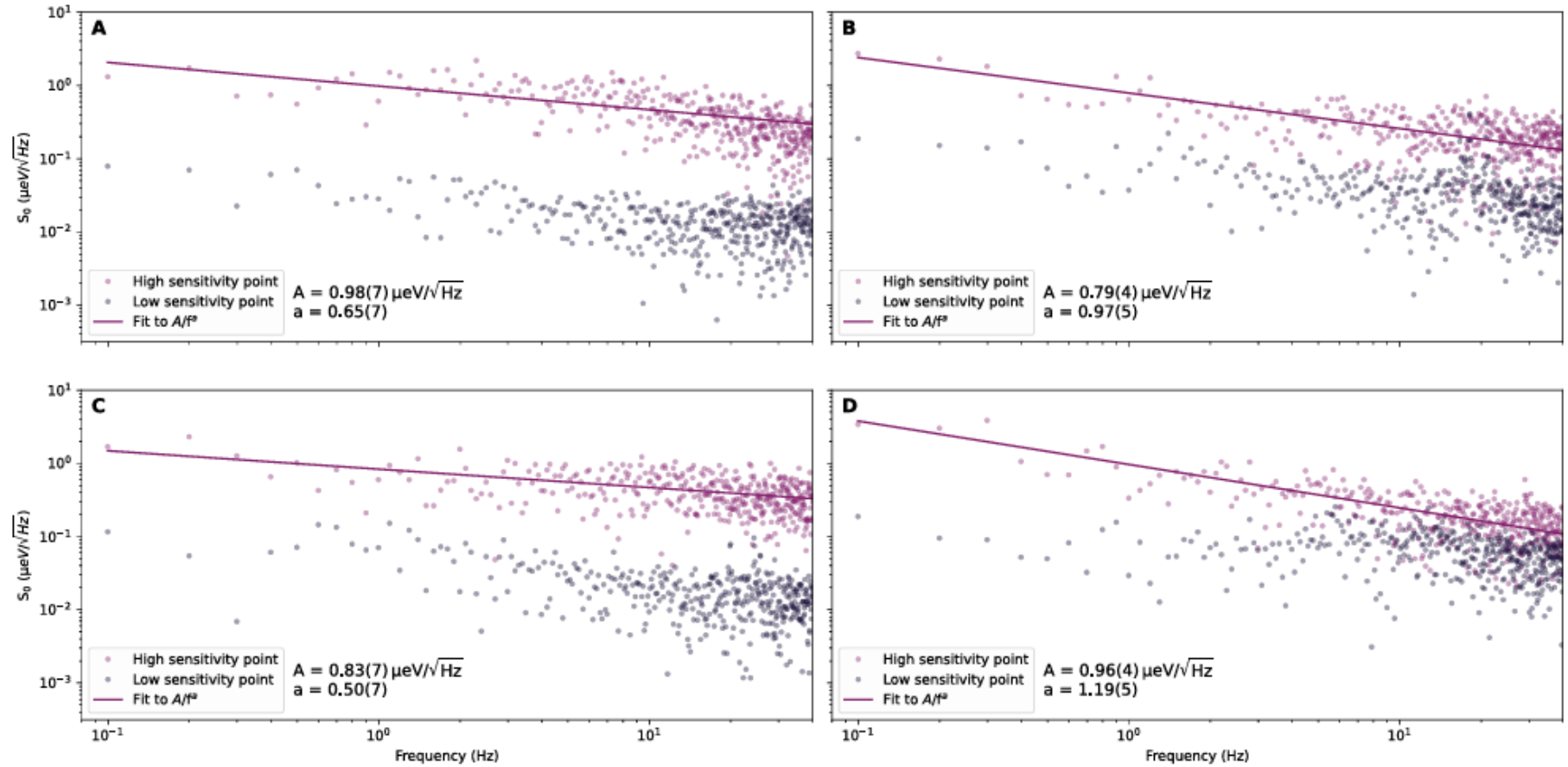


The Pauli spin blockade at the (3,1)–(4,0) charge transition was used for spin parity read-out

SET– Charge noise spectrum



Coulomb peaks



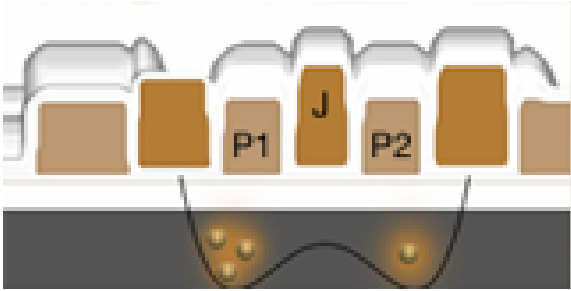
Charge noise spectrum of device A, B, C and D

SET charge-noise measurements reveal $\frac{A}{f^a}$ power spectral density

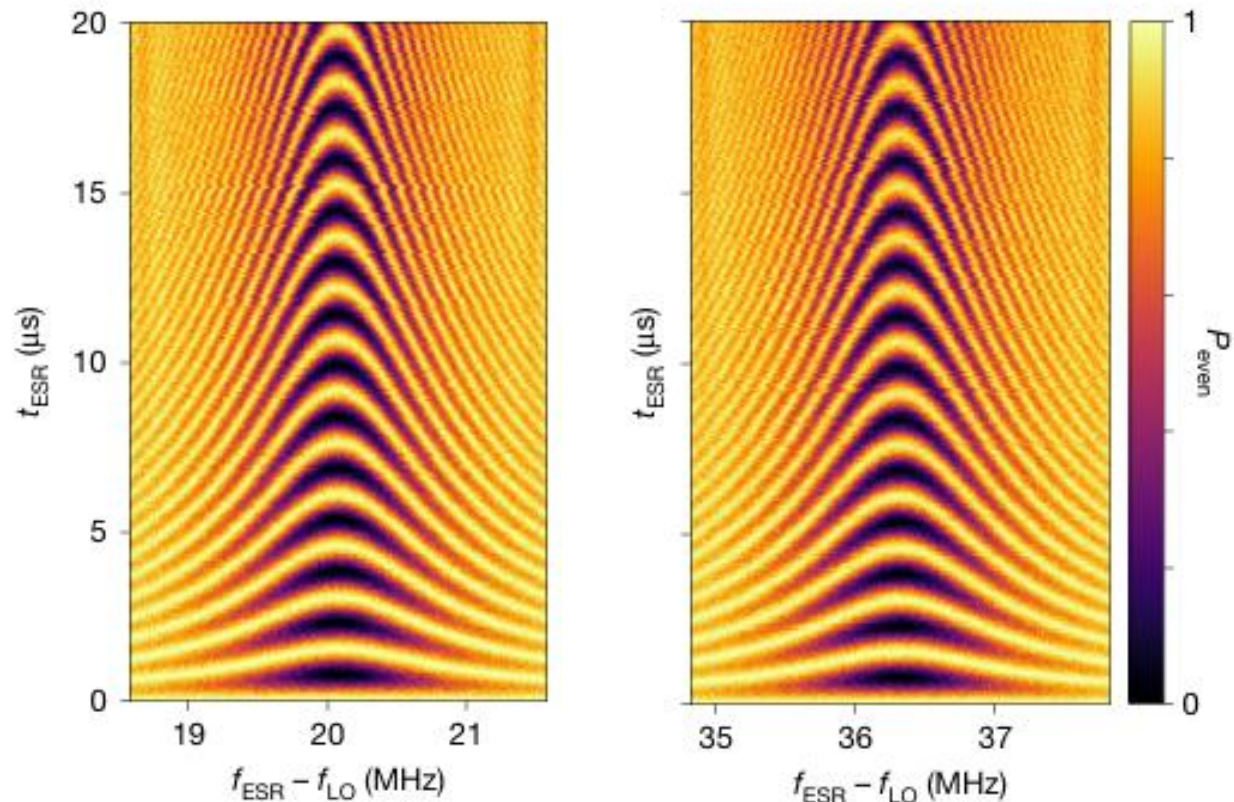
'a' $\rightarrow$ 0.50(7) - 1.19(5)

amplitude $A \rightarrow$ 0.79(4) - 0.98(7) $\mu\text{eV}/\text{Hz}$ at 1 Hz

Single qubit gate operation



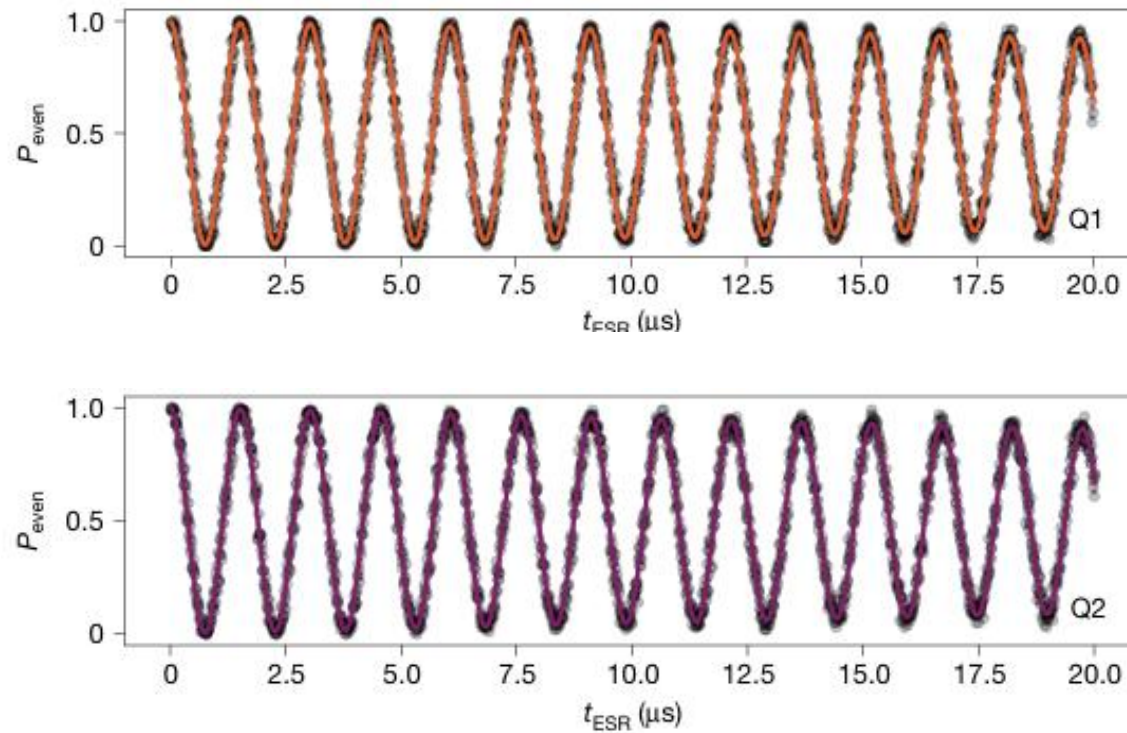
- $B = 0.662\text{--}0.7\text{ T}$ split the spin states to form the single-qubit states
- manipulated with microwave signals applied to the ESR antenna with frequency f_{ESR}
- Applying microwave signal at the frequency $f_{\text{ESR}} - f_{\text{LO}}$ for a duration of t_{ESR} gives the Rabi chevron pattern for the qubit Q1 and Q2.
- **Single-qubit $X_{\frac{\pi}{2}}$ gates** formed with timed microwave pulses on resonance with the qubit Larmor frequencies f_{Q1} and $f_{Q2} \rightarrow$ **rotate the qubit to the equator**
- **$Z_{\frac{\pi}{2}}$ gates** were implemented as virtual gates through rotations of the reference frame



Rabi chevron of Q1 and Q2

$$f_{\text{LO}} = 18.610\text{GHz}$$

Rabi oscillations

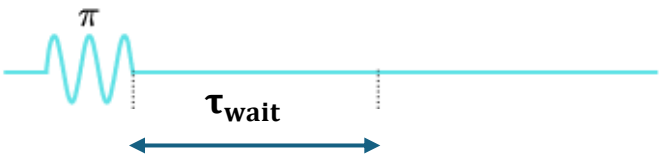


$$f_{\text{Rabi}} = 658.6(3) \text{ kHz}$$

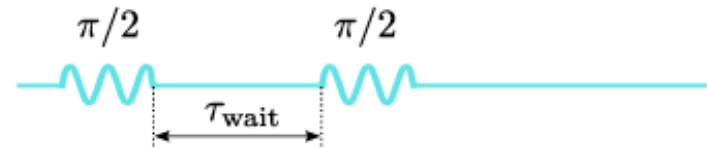
7% more power on Q1 to match the rabi frequency of both the qubits

Qubit lifetime

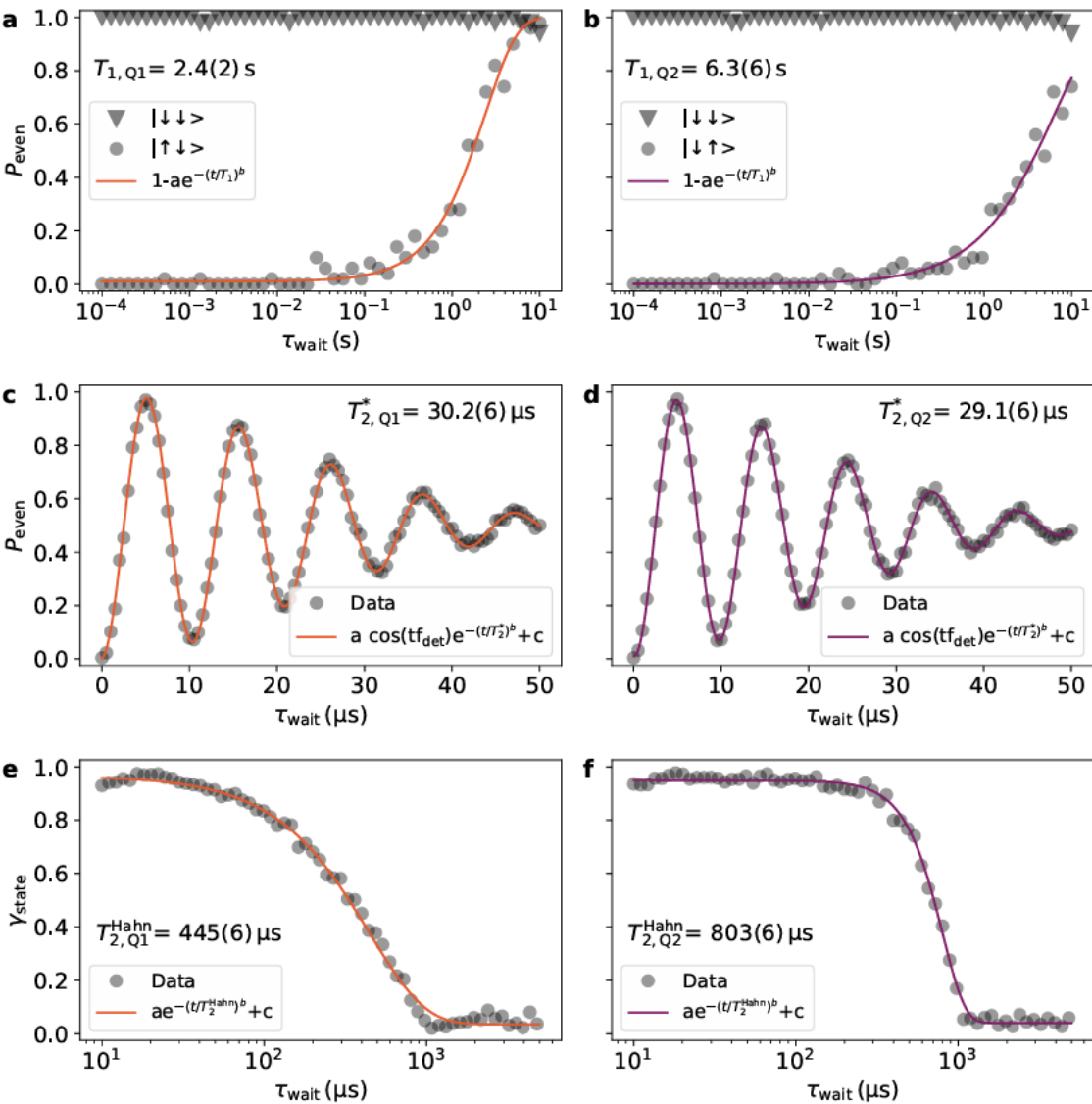
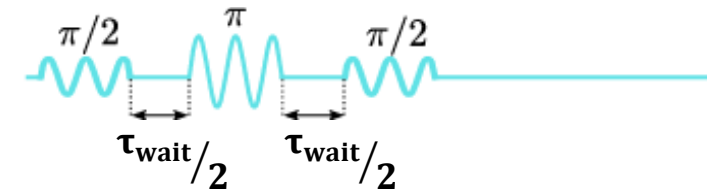
Relaxation time()



Ramsey

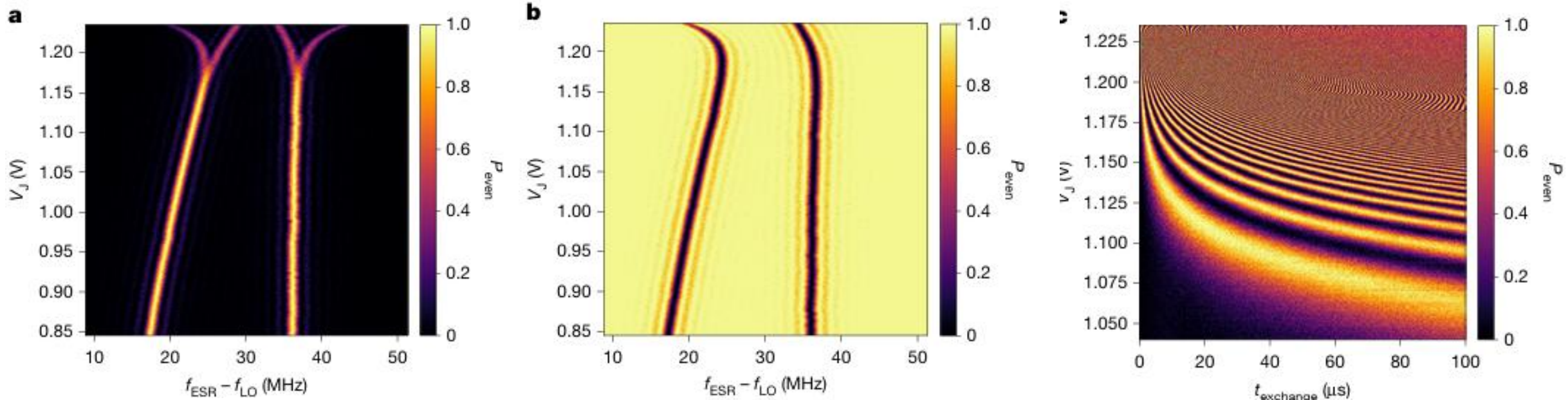
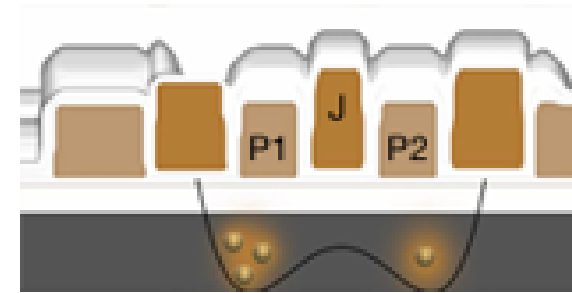


Hahn echo



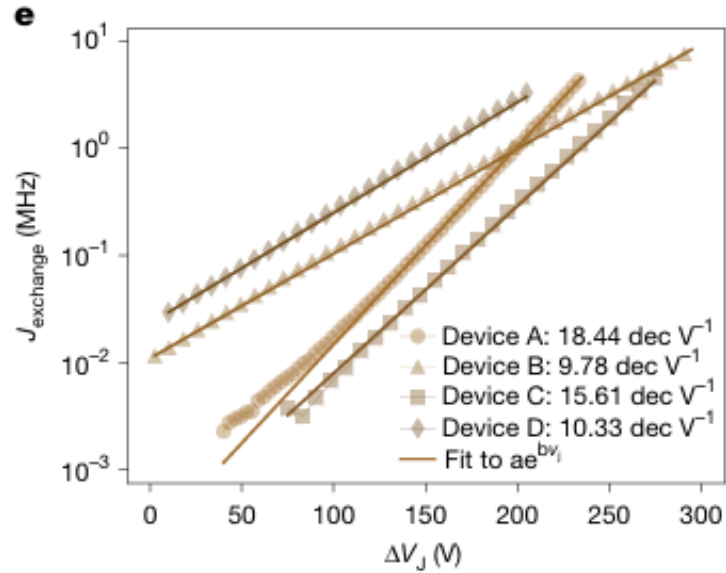
2 qubit gate implementations

To implement two qubit control J gate has to be tuned

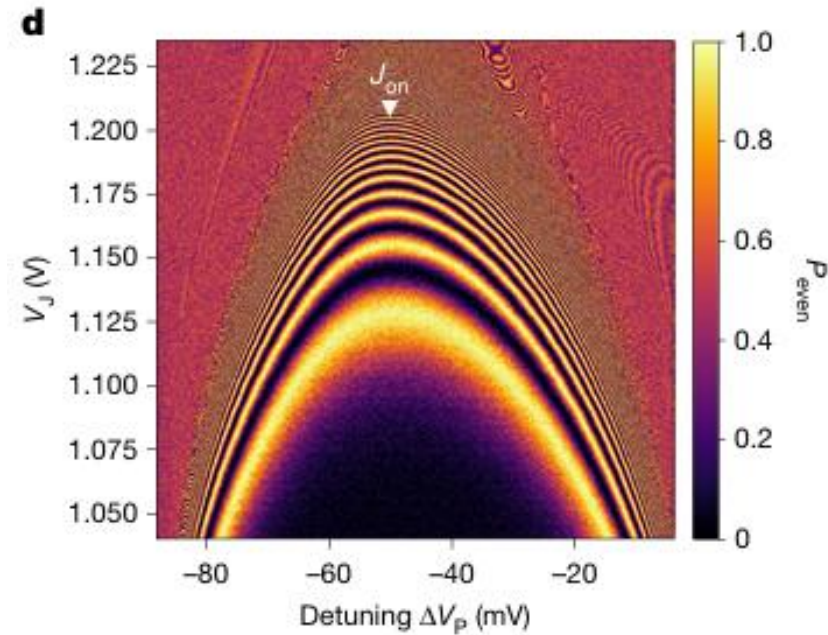


Pulsed exchange interaction combined with single-qubit phase rotations (to filter out phase-accumulating effects), controlled-Z (CZ) two-qubit gate is implemented

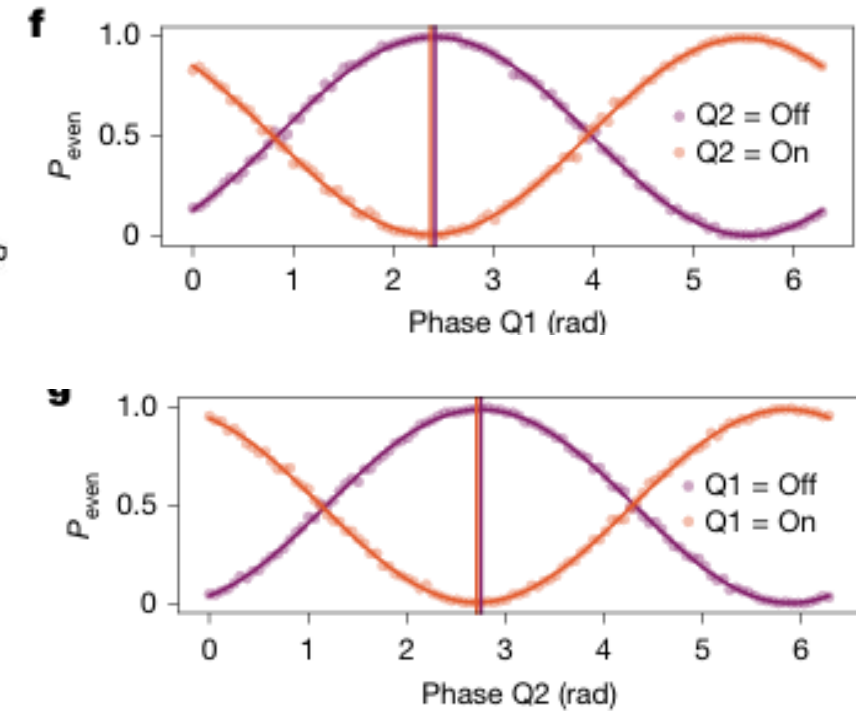
CZ gate calibration



- Exchange strength Vs exchange gate voltage
- extracted from fitting exchange oscillations
- assuming $J_{\text{exchange}} \propto a e^{bV_J}$
 $b = 9.78 \text{ dec } V^{-1}$ and $18.44 \text{ dec } V^{-1}$

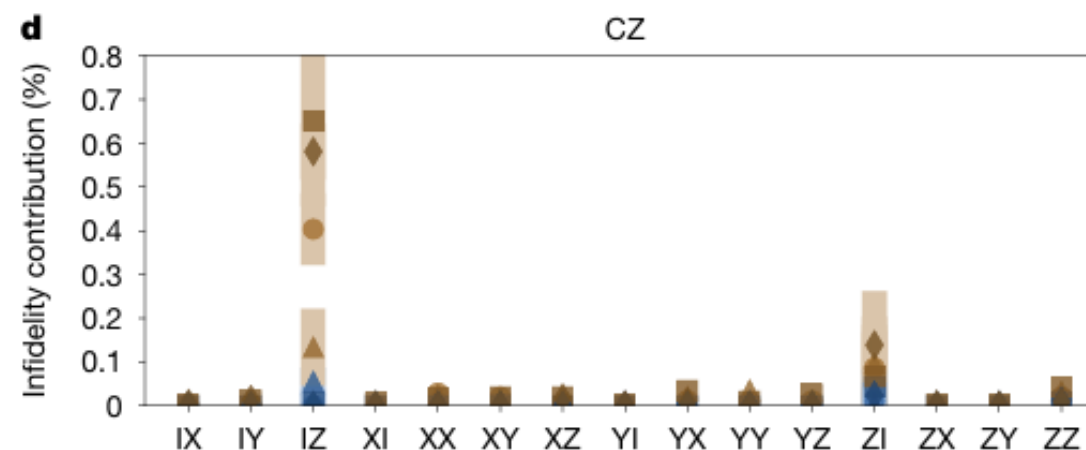
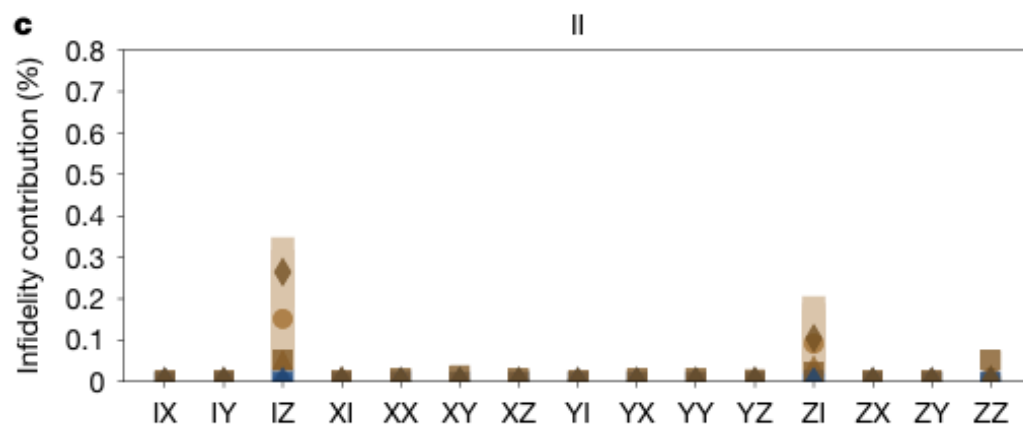
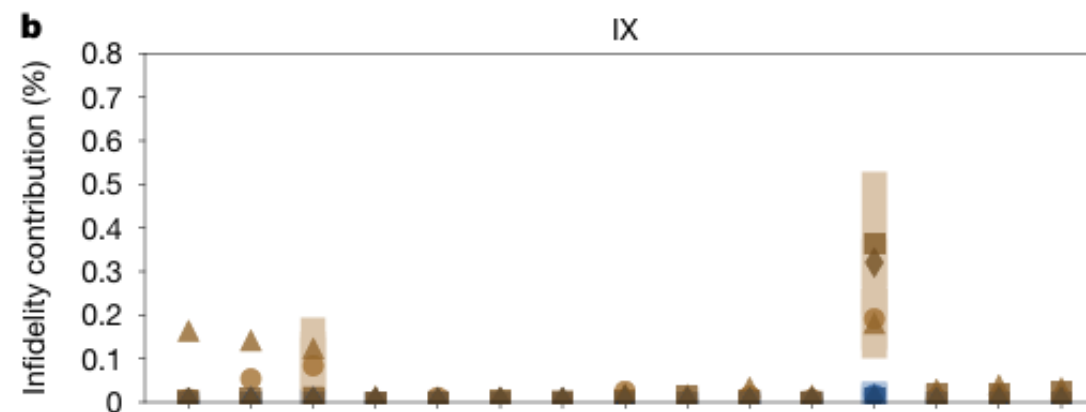
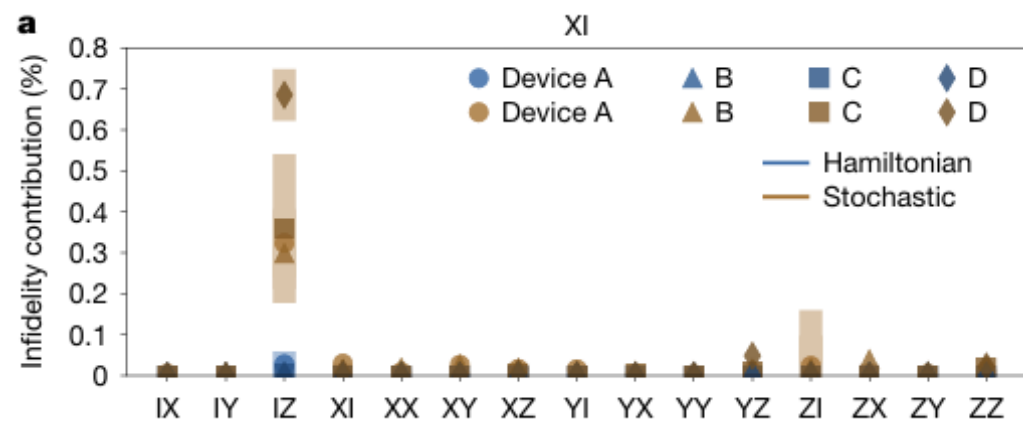


symmetric charge operation point to reduce the sensitivity to the detuning noise



- **Calibration of the CZ single-qubit phase correction**
- Prepare in superposition, applying a CPHASE followed by a virtual phase rotation for each qubits
- Vertical lines indicate the phase values for which the spin state of Q1 (Q2) is flipped if Q2 (Q1) is in the on/spin-up state

Two qubit benchmarking using GST(gate set tomography)



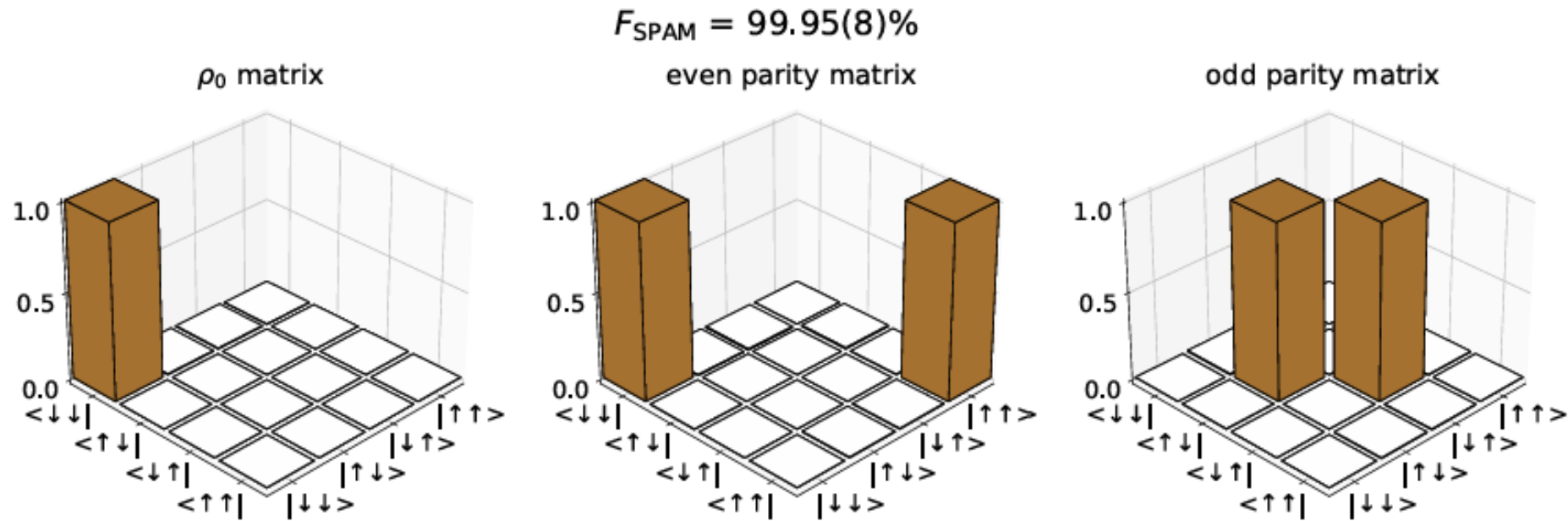
Key notes

- IZ(ZI) infidelity is due to small time delay in the control hardware

Error mechanism

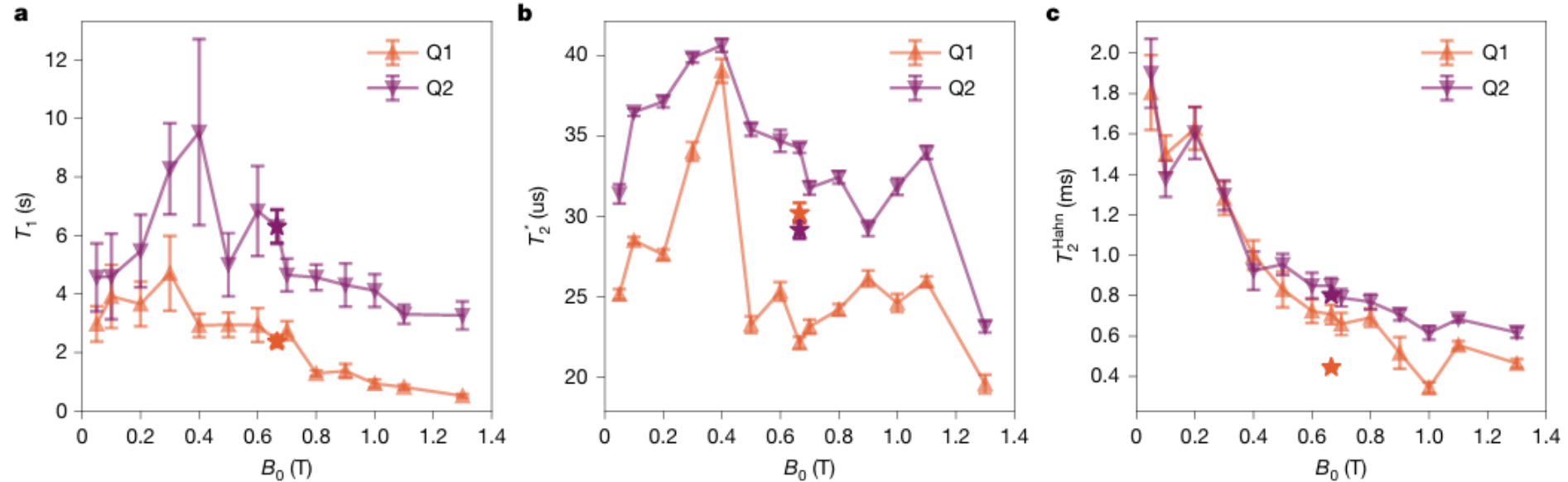
- Electron spin states coupled to the residual nuclear spin states

State preparation and measurement(SPAM)



Initialization Fidelity = 99.996%
Measurement Fidelity = 99.959%
Combined SPAM = 99.95%

Qubit lifetime magnetic field dependance



- At large B stronger coupling to charge noise through the spin–orbit interaction and resulting in reduced coherence is seen.
- the B field points in the $[110]$ lattice orientation, where the variability of the g factor is highest and the Dresselhaus spin–orbit component dominates.

Table 1 | Device performance reproducibility

Device	B_0 (mT)	Fidelity (%)					T_1 (s)		T_2^* (μ s)		T_2^{Hahn} (μ s)	
		SPAM	XI	IX	II	CZ	Q1	Q2	Q1	Q2	Q1	Q2
A	666	99.95(8)	99.48(5)	99.55(4)	99.74(9)	99.37(5)	2.4(2)	6.3(6)	30.2(6)	29.1(6)	445(6)	803(6)
B	662	99.33(9)	99.47(6)	99.18(5)	99.89(9)	99.56(6)	0.9(2)	0.8(1)	30.5(2)	26.2(2)	811(24)	148(4)
C	700	99.97(22)	99.59(15)	99.51(14)	99.81(6)	99.04(16)	1.3(2)	1.9(2)	34.2(1.1)	32.5(2.3)	1,569(56)	1,044(52)
D	700	99.96(5)	99.23(3)	99.64(3)	99.62(6)	99.20(3)	1.8(2)	0.12(1)	21.5(4)	9.3(1)	357(15)	118(2)

Operation fidelities of four nominally identical devices from the same 300-mm wafer benchmarked using GST. Spin lifetime and coherence metrics across devices are obtained following Extended Data Fig. 2. Errors are based on the 95% confidence level.

Take Away messages

- High-fidelity silicon qubits demonstration using **standard 300-mm silicon manufacturing lines** to scaling to millions of qubits on a single chip.
- Demonstrated long qubit lifetimes with $T_1 \sim 9.5\text{secs}$, $T_2^* \sim 40.6\mu\text{s}$ and $T_2^{\text{Hahn}} \sim 1.9\text{ms}$
- Dominant remaining errors actually stem from **residual nuclear-spin isotopes** left in the silicon lattice.

Fig. 2 | SET operation and device uniformity.

a The SET device structure. The top is the SEM top view. The barrier gates have a critical dimension of 30 nm with a space of 60 nm. At the white dashed line, the schematic cross section is shown in the middle. The bottom shows the conduction band edge diagram, where the SET top gate (ST) forms the electron channel and the left and right barrier gates (LB and RB) induce the barriers above the Fermi level and define the quantum dot. **b** Barrier gate stability map at a fixed $V_{ST} = 3.5$ V. The single quantum dot between the barriers gives the diagonal Coulomb oscillation lines in the map (white dashed lines). **c** $I_D V_G$ characteristics of the top gate (blue lines) and barrier gates (green lines) across 12 SETs at 10 mK. **d** The cumulative distribution functions (CDF) of the threshold voltage (V_{TH}) and sub-threshold swing (SS) of the SET gates. The almost vertical lines, especially for the barrier gates, highlight the level of uniformity with advanced manufacturing techniques.

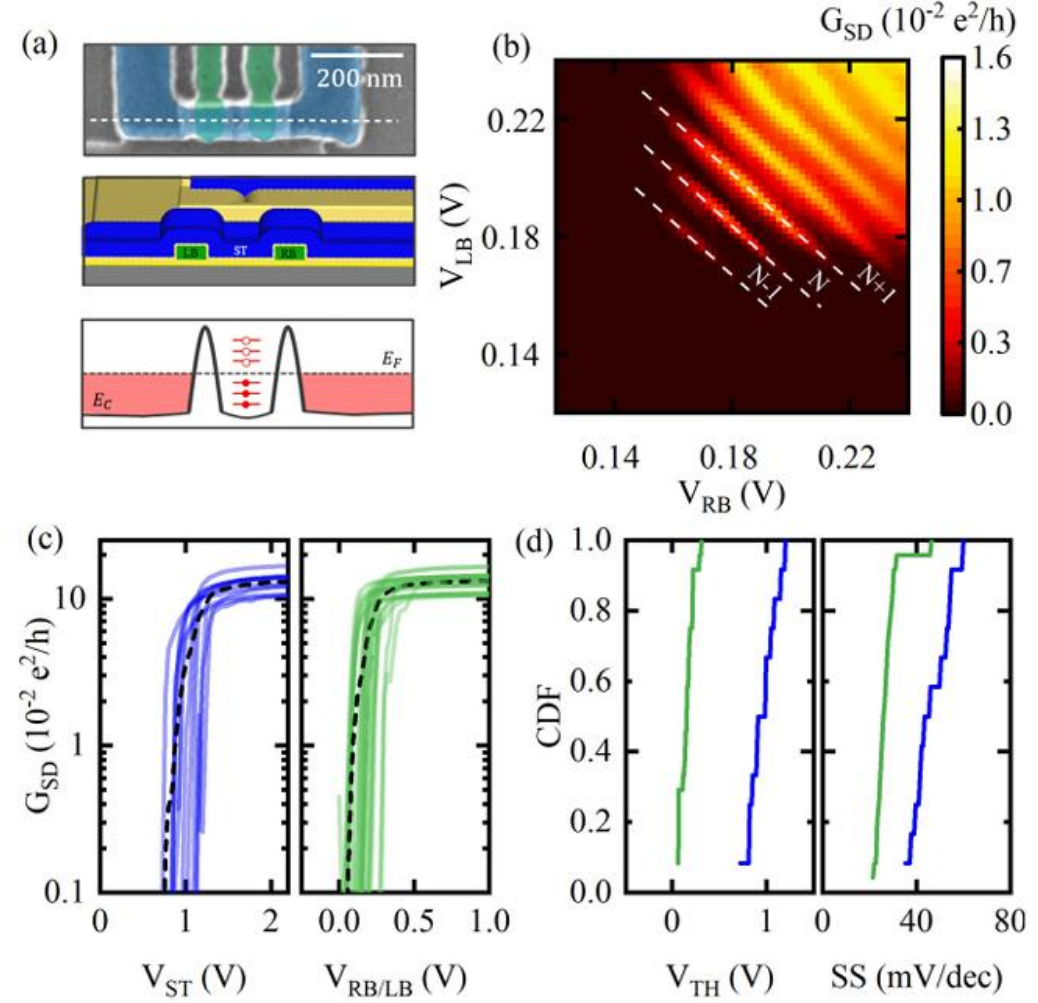


Fig. 3 | SET current spectroscopy and device statistics. **a** Noise spectral density of the quantum dot. The resulting spectrum of the average of all 223 measurements showing a standard $1/f$ spectrum (blue) showing a standard $1/f$ spectrum. Spectral density of the charge noise in Coulomb blockade (orange) highlights that the background noise does not limit the measurements. The noise spectrum of one of the lowest charge noise spectra measured on Device H (red). **b** Coulomb oscillations of device A (black) by sweeping the ST bias. The charge noise at different peaks is overlaid. **c, d** The violine plot of S_0 and γ across 12 SETs and 223 peaks, with the mean value shown as a solid line.

