Overview

The course was divided into:
- Semiconductor e-Detector
- Characteristics
  - Conductance type $n \leftrightarrow p$
  - Temperature dependence of resistance
  - Hall measurement
  - Specific resistance
  - Lifetime of charge carriers
- Dry Etching
- MOSFET-Fabrication
  - Basics of MOSFETs
  - Fabrication
  - Result
Conductance type $n \leftrightarrow p$

- Heat gradient
- Different chemical potential
- Charge carriers diffuse

Type-dependent polarity:
- Hot tip positive: n-type
- Hot tip negative: p-type
Temperature-dependent Resistance

- **Basically:** \( \rho = \rho(T), \ \mu = \mu(T), \ \sigma = e\rho\mu \)

- **Undoped Si:**
  - \( T=0 \): no charge carriers, \( \sigma = 0 \)
  - \( T>0 \), e jump to valence band, \( \sigma \uparrow \)
  - \( T>>0 \), lattice oscillations, \( \sigma \downarrow \)

- **Doped Si:**
  - \( T\approx0...150K \): no intrinsic cc, no ionized dopants
  - \( T \approx 150K...450K \): all dopants ionized, no intrinsic cc
  - \( T>450K \): intrinsic cc exceed dopants

- **Measurement:** flow cryostat
Specific Resistance

- Metal-SC-contact:
  Schottky barrier = nonohmic/nonlinear

- 4-tip-method:
  - branded current
  - Measure voltage drop
  - consider particular geometry
Life Time of CC

- Formation of CC through energy (thermal, light, ...)
- Recombination after life time $\tau$
  - Expose Si to light
  - CC propagate
  - Switch off light
  - CC recombine
  - $\sigma$ decays exponentially
  - Problem: finite rise/decay time of light exposition

$\tau = \frac{t_{1/2}}{\ln 2}$

$\rightarrow$ Source of Noise
Dry Etching I

Etching rate in dependence of $c(O_2)$

- $CF_4$: 30sccm
- $P_{rf}=100W$
- $t=10min$
- $p=100mtorr$

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<tr>
<td>$C(O_2)$</td>
<td>0%</td>
<td>20%</td>
<td>40%</td>
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<td>$d/nm$</td>
<td>376</td>
<td>2411</td>
<td>836</td>
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Dry Etching II

Etching rate and side characteristics in dependence of p

- CF₄: 30sccm  t=10min
- O₂: 8sccm  P₀rf=100W

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<th>III</th>
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<tr>
<td>p/mTorr</td>
<td>20</td>
<td>100</td>
<td>130</td>
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<td>d/nm</td>
<td>177</td>
<td>922</td>
<td>1464</td>
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Dry Etching III

Etching rate and side characteristics in dependence of $c(\text{CHF}_3)$

- $\text{CF}_4$: 20 sccm
- $\text{O}_2$: 4 sccm
- $t=10\text{min}$
- $p=100\text{mtorr}$
- $P_{\text{rf}}=100\text{W}$

<table>
<thead>
<tr>
<th>$c(\text{CHF}_3)$</th>
<th>0%</th>
<th>25%</th>
<th>35%</th>
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<tr>
<td>$d/\text{nm}$</td>
<td>2317</td>
<td>426</td>
<td>353</td>
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Dry Etching IV

Goal: trench $1\mu$m, vertical edges

- $\text{CF}_4$: 60%  $t=10\text{min}$  $p=100\text{mtorr}$
- $\text{O}_2$: 8%  $\text{CHF}_3$: 32%  $P_{\text{rf}}=100\text{W}$

→ see thermographic print out
MOSFET
Metal Oxide Silicon Field Effect Transistor

Basics
nnpn-type
Start with pre-p-doped (Boron) Si-wafer, preliminary SiO₂-Layer, thermal grown, 250nm, 1150°C, dry O₂

2. Spinning cycle:
   - Dehydration: hotplate, 5min, 180°
   - Spinning resist ma-P 215S: 5s at 2000rpm + 40s at 4000rpm
   - Prebake: evaporate solvant, 3min, 90°C

3. Light exposition 25s

4. Developping: maD-371: s40s slow turning, flush with H₂O, blow with N₂

5. Edging alignment markers: buffered HF, 3:15min, hydrophilic (SiO₂)→hydrophobic (Si)

6. Cleaning cycle:
   - Acetone
   - Flushing
   - Blowing

7. Edging markers in Si: 10% KOH, 70°C, 20min, stopped by flushing

8. Spinning cycle
MOSFET

Metal Oxide Silicon Field Effect Transistor

9. Expose for source and drain
10. Developping
11. Hardbake: 120°C, 3min
12. Edging source and drain areas in SiO₂, see 5.
13. Remove remaining resist, cleaning cycle
14. Diffusion: PDS phosphorus wafer, 30min, 93°C, N₂ atmosphere
15. Remove damaged oxide: buffered HF again
16. Oxidation (thin layer): 850°C, 30min
17. Spinning cycle
18. Expose for source and drain contact areas (SDCA)
19. Developping
20. Uncover SDCA: buffered HF, 48s
MOSFET
Metal Oxide Silicon Field Effect Transistor

21. Spinning cycle
22. Expose for contacts
23. Evaporation
   i. 10nm Titanium
   ii. 40n Silver
24. Lift-Off

→Measure characteristic curves!
MOSFET
Metal Oxide Silicon Field Effect Transistor

What they **should** look like:
MOSFET
Metal Oxide Silicon Field Effect Transistor

What they **do** look like: