Supplementary Material: Self-aligned gates for scalable silicon quantum computing

Simon Geyer,[1] Leon C. Camenzind,[1] Lukas Czornomaz,[2] Veeresh Deshpande,[2,*] Andreas Fuhrer,[2] Richard J. Warburton,[1] Dominik M. Zumbühl,[1,†] and Andreas V. Kuhlmann[1,2,‡]

[1]*Department of Physics, University of Basel, Klingelbergstrasse 82, CH-4056 Basel, Switzerland*
[2]*IBM Research-Zürich, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland*

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S1. ELECTRICALLY ISOLATION OF THE TWO GATE LAYERS

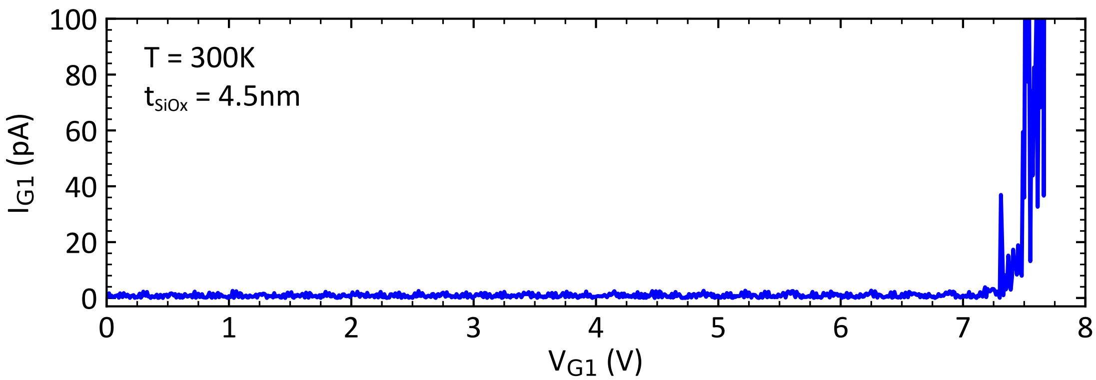

Fig. S1. The two gate layers are electrically isolated by a thin SiO_x layer of $t_{SiOx} \simeq 4.5$ nm thickness, measured by ellipsometry. The oxide is deposited by means of atomic layer deposition, allowing for a monolayer control of t_{SiOx}. A typical oxide breakdown curve is presented in the above figure, where the current flowing between the two gate layers is plotted while sweeping the voltage difference between them. Here, oxide breakdown occurs for a voltage difference >7 V, corresponding to a breakdown field strength of 16 MV/cm. While the measurement is performed at room temperature, impurity freeze-out at cryogenic temperatures will shift the breakdown point to higher voltages.

* Current address: Institute IFOX, Helmholtz Zentrum Berlin für Materialien und Energie, Hahn-Meitner Platz 1, D-14109 Berlin, Germany
† dominik.zumbuhl@unibas.ch
‡ andreas.kuhlmann@unibas.ch

S2. SINGLE- AND DOUBLE DOT OPERATION MODE

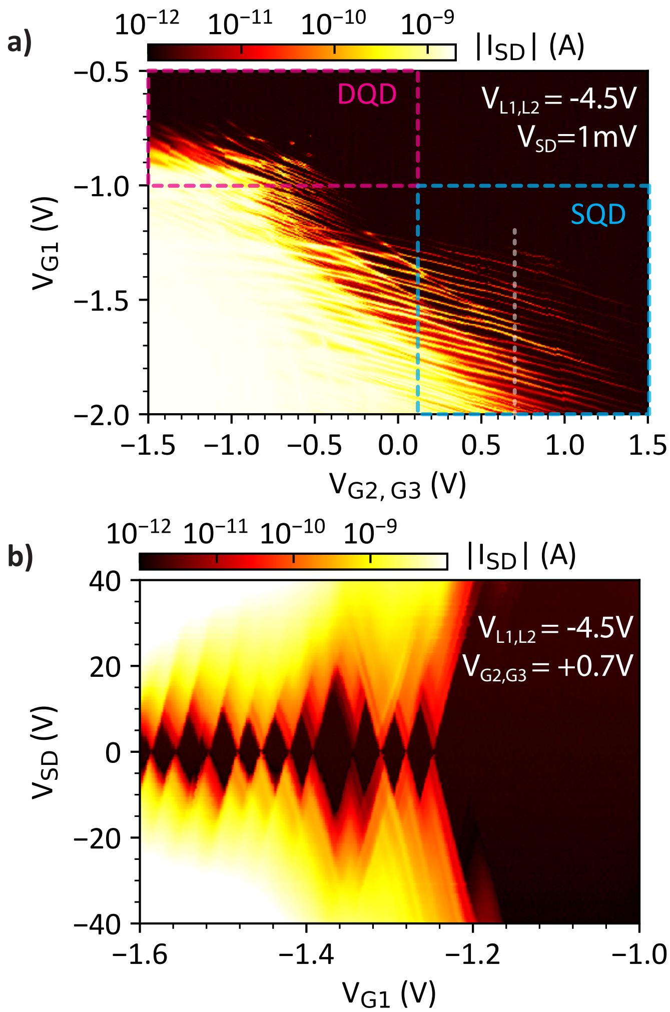

Fig. S2. The device gate layout allows for a dual-mode operation as single (SQD) or double quantum dot (DQD). A map of source-drain current I_{SD} as a function of $V_{G2,G3}$ (same voltage applied to both gates) and V_{G1} is presented in (a). The SQD regime is located in the bottom right corner of this map: a positive voltage applied to gates G2 & G3 induces tunnel barriers to source and drain reservoirs, and the voltage applied to gate G1 forms the dot and controls its occupancy. In this regime Coulomb oscillations are observed along the V_{G1} axis. A single dot charge stability diagram for $V_{G2,G3} = +0.7\,V$, marked by the white dashed line in (a), is shown in (b). Clear Coulomb diamonds are observed and the their closing at zero bias suggests the formation of a SQD. The less positive $V_{G2,G3}$ the more transparent the barriers to source and drain become. In the top left corner of (a) the device is operated as a DQD. Gates G2 & G3 are at negative voltages and accumulate holes, while gate G1 is at more positive voltages and creates the inter-dot tunnel barrier.

S3. TUNING OF THE INTER-DOT TUNNEL COUPLING WITH GATE G1

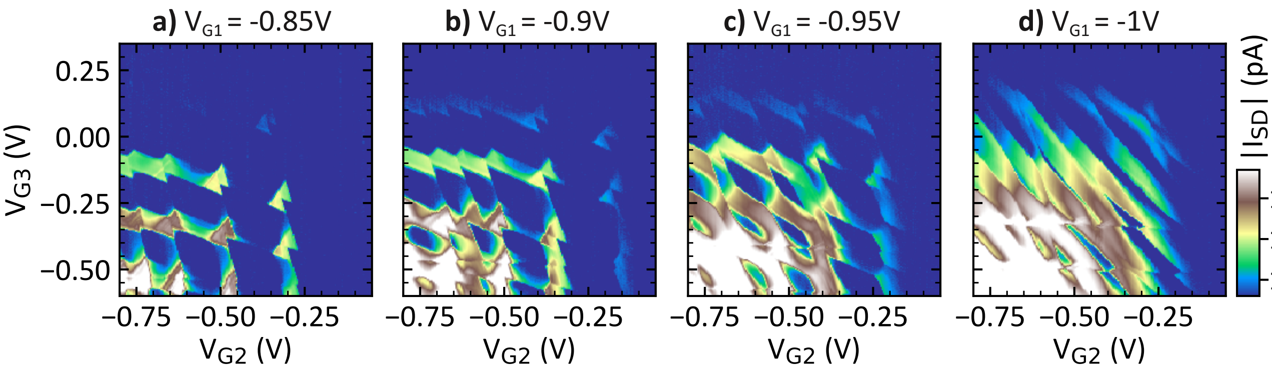

Fig. S3. Charge stability diagrams for different values of voltage applied to the central nanogate G1. By decreasing V_{G1} the inter-dot tunnel coupling is increased, as evident from the transition from a double quantum dot (a) to a more single-dot-like configuration (d). Data were taken at $V_{SD} = -5\,\mathrm{mV}$ and $V_{L1,L2} = -4.5\,\mathrm{V}$.

S4. CHARGE STABILITY DIAGRAM OF A SIMILAR DEVICE

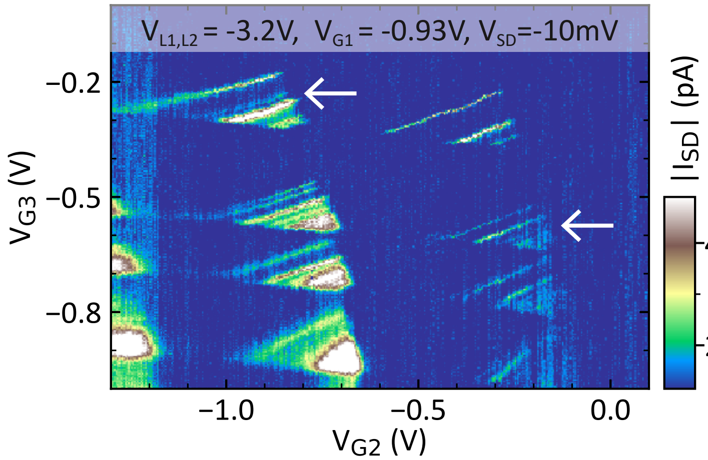

Fig. S4. Double dot charge stability diagram of a device that is similar to the one discussed in the main article. While the devices share a common plunger gate length of $\simeq 15\,\mathrm{nm}$, they differ in the inter-dot barrier length: here $\simeq 35\,\mathrm{nm}$ instead of $\simeq 25\,\mathrm{nm}$. The wider barrier leads to a current reduction. The pairs of bias triangles are arranged in a very similar way to Fig. 2 (a) of the main article. Again, signatures of Pauli spin blockade are observed for the bias triangles indicated by the white arrows. The high degree of similarities between the data presented in here and the main article demonstrates that reproducible double dot formation is achieved.

S5. SPIN BLOCKADE FOR $(1,1) \leftrightarrow (2,0)$ CHARGE TRANSITION

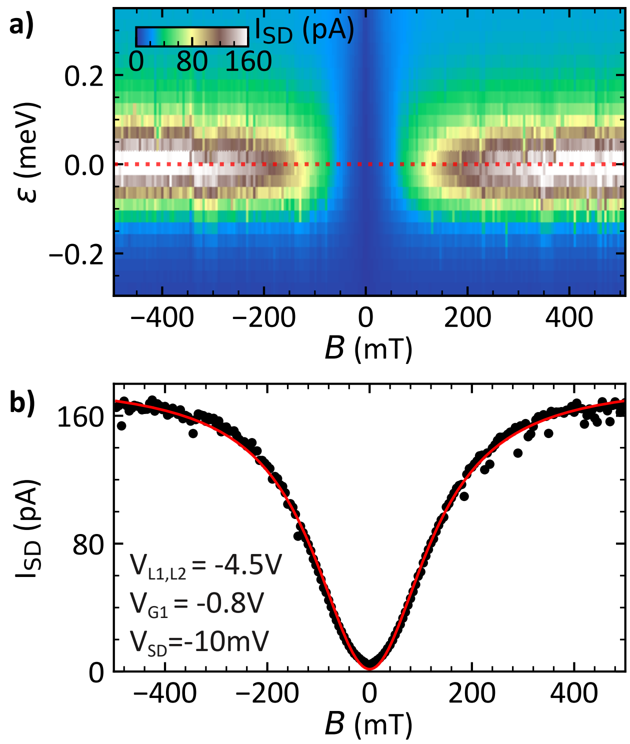

Fig. S5. Analogue to Fig. 3 of the main article for the pair of bias triangles highlighted by a solid magenta circle in Fig. 4 (a) of the main article, corresponding to $(1,1) \leftrightarrow (2,0)$ charge transitions. As expected current suppression due to spin-conserved tunneling is now observed for negative V_{SD}, i.e. the opposite bias direction compared to the data presented in the main article. A cut along B at zero detuning reveals again a dip in the leakage current, indicating that spin blockade lifting is dominated by SOI. This dip has a Lorentzian lineshape with FWHM = 270 mT.