Spin Qubits in Silicon FinFET Devices

A. Fuhrer[1], M. Aldeghi[1], T.Berger[2], L. C. Camenzind[2], R. S. Eggli[2], S. Geyer[2], P. Harvey-Collard[1], N. W. Hendrickx[1], E.G. Kelly[1], L. Massai[1], M. Mergenthaler[1], P. Müller[1], A. V. Kuhlmann[1,2], T. Patlatiuk[2], S. Paredes[1], F. J. Schupp[1], G. Salis[1], L. Sommer[1], K. Tsoukalas[1], N. Vico Trivino[1], R. J. Warburton[2], D. M. Zumbühl[2]
[1]IBM Research Europe - Zurich, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland, email: afu@zurich.ibm.com
[2]Department of Physics, University of Basel, Klingelbergstrasse 82, CH-4056 Basel, Switzerland

2022 IEEE International Electron Devices Meeting (IEDM) | 978-1-6654-8959-1/22/$31.00 ©2022 IEEE | DOI: 10.1109/IEDM45625.2022.10019477

***Abstract* —** We discuss a custom bulk FinFET platform for implementing fast and dense hole spin qubits. Using a double quantum dot with two confined holes, single- and two-qubit control is demonstrated by applying electrical microwave signals to one of the gate electrodes. From these experiments we estimate that both types of gate operations can be realized with gate times in the few nanoseconds regime. In an outlook we discuss how to further scale this technology towards 2D arrays.

I. Bulk FinFET Platform for Silicon Spin Qubits

Silicon CMOS devices have been the workhorse for classical electronic device scaling for several decades. More recently, applications in the quantum computing domain e.g. for ultra-low power cryogenic control electronics and the realization of spin qubits in isotopically purified silicon, have attracted significant attention. This has led to the application of standard CMOS platforms to these new application fields [1–3]. Using a standard technology platform has the key advantage of directly leveraging years of technology improvements for classical CMOS devices, but it also bears the risk that some of the optimization targets for these devices are not suitable for spin qubits at cryogenic temperatures. Furthermore, existing bounds such as design rules and set material choices may severely limit the flexibility and speed with which required adaptations can be implemented in such standard processes.

Instead, we have developed a dedicated bulk FinFET process that avoids the presence of dopants near the quantum dots, uses a high-quality thermal silicon oxide as a gate dielectric and is based on bulk intrinsic silicon such as to avoid additional interfaces from a buried oxide and to allow for a simpler implementation of a process with isotopically purified materials (see Fig. 1) in the future. All patterning is done using high-resolution electron beam lithography. The fin cross-section is chosen to be triangular and charge carriers are confined electrostatically by gates wrapping around the fin. Contacts are formed using a silicide Schottky contact and a contact gate that accumulates charge carriers from the contact to the quantum dot devices. The choice of the silicide may favor one device polarity (electrons or holes) but in contrast to degenerately doped contacts, device polarity can be determined by the sign of the voltage applied to the contact gates [4]. Fig. 1 b) shows a device with a single titanium nitride gate layer, where the quantum dot is formed below a plunger gate (B) and the barriers are induced by the ungated intrinsic regions between the contact gates and the plunger gate.

A. Short-loops for device characterization

To characterize basic material and processing parameters such as density, mobility, capacitance, and gate isolation, we use dedicated Hall bar, MOS capacitor, and large channel transistor devices based on the same gate stack (see Fig. 2). They allow separation of contact resistance from channel properties and have no features with critical dimensions below a micron. These devices can thus be fabricated with standard optical lithography facilitating fast turn-around and rapid parameter feedback.

B. Contact Resistance

Using nickel silicide as a contact material allows for ambipolar operation of a quantum dot device simply by tuning the voltage on the contact gates [4]. However, the dramatic increase of contact resistance at low temperature and low source-drain bias makes it challenging to use such contacts for near-term cryogenic transport experiments. For this, a contact resistance smaller or similar to the resistance quantum (h/e^2) is important, because many of the techniques used in Coulomb blockade transport spectroscopy rely on the applied bias voltage as an accurate measure for the voltage drop across the quantum dot itself and not the contacts.

To address this issue, we used platinum silicide as a contact material for holes (lower Schottky barrier height) and implemented a separate gate just for tuning the Schottky barrier (see Fig. 3). In this case, the silicide anneal occurs before the deposition of the gate stack for these Schottky gates and allows the use of e.g. high-k gate dielectrics. Still, we find that the high Schottky gate voltages needed for low resistance contacts can lead to fluctuating device currents, which make it hard to measure devices reliably in transport. Therefore, we also developed a process for in-situ doping of the contact areas with highly boron-doped polysilicon. This results in fully Ohmic contact behavior down to cryogenic temperatures and contact resistances in the required range (see Fig. 3d)).

C. Self-aligned second gate layer

Another limitation of the simple device arrangement shown in Fig. 1 b) is the fact that the fin surfaces between the gate electrodes are exposed to ambient conditions after definition of the gate electrodes by etching. Furthermore, the potential barrier that confines the quantum dots is very sensitive to local charges between the gates, and local electrode roughness,

leading to inconsistent formation of quantum dots (see Fig. 4). This was improved significantly by implementing a second gate layer for increased tunability of the confinement potential [5]. This second gate layer does not require additional high accuracy alignment. It is formed in a self-aligned fashion between the gates of the first metal layer and is insulated by a thin silicon dioxide dielectric. It allows for more tunability and screens disorder from charges between the gates of the first gate layer. Furthermore, it allows a choice of whether to define the quantum dots below the first gate-layer gates or below the gates of the second gate layer. The latter allows for the definition of a double quantum dot in a very simple device such as the one in Fig. 1 b) and Fig. 5 a).

II. Hole Spin Qubit Operation

The strong spin-orbit interaction for hole spins in silicon [6] allows for all-electrical spin control simply by applying a microwave electric field through one of the gates close to the quantum dot [7–9]. This strong coupling of the electric field to the spin enables ultra-fast qubit manipulation speeds [10–12] up to several hundred megahertz. However, it also couples the spin degree of freedom directly to charge- and electric-field noise present in all semiconductor devices. Typically, this results in a short coherence time but the recent discovery [13] and first experimental demonstration of charge-noise sweet spots [14] may allow to overcome this challenge and make hole spins a very attractive platform for silicon-based quantum computing. In the following we focus on a double quantum dot as shown in Fig. 5 a), defined by accumulating a hole spin below each of the second gate layer gates (P1, P2) and using the first gate layer plunger gate (B) to tune the potential barrier between the qubits.

A. Spin read-out

For read-out of the spin state, we use Pauli spin blockade (PSB). Here, transfer from a (1,1) charge configuration in the double quantum dot to a (0,2) configuration is only energetically allowed if the two spins can form a singlet, effectively converting the spin state into a charge state and allowing read-out either with charge-sensing or dispersive gate sensing. For our qubit experiments we have used a transport-based read-out scheme where the experiment is continuously repeated and spin-selective transfer of the charge between the two dots leads to a difference in the measured current. Faster and more sensitive read-out requires integration of resonators either off-chip or on-chip, an effort that is currently ongoing (see Fig. 4).

B. Single-Qubit Operations

For single qubit operation we initialize the double quantum dot in a $|\uparrow,\uparrow>$ state by waiting long enough for transport to be blocked by PSB. Then the potential on (P1) is lowered to move into a Coulomb blockade situation where a microwave pulse (see Fig. 5 b)) is applied to the same gate (P1). Finally the potential on (P1) is again increased and if one of the spins has been rotated to form a $|\uparrow,\downarrow>$ state, charge can be transferred to S(0,2). When the experiment is continuously repeated, a small current difference is detected. This allows the observation of Rabi oscillations as shown in Fig. 5 c). In a similar way a Ramsey experiment can be realized such as the one shown in Fig. 5 d). Note, that this scheme does not require any additional ESR-lines or micromagnets, but the control signals are directly applied to the existing gate electrodes. This allows for a very dense architecture.

C. Tunable Exchange Gate

Exchange interaction between two hole spins can serve as a fast and scalable two-qubit gate [15]. One of the challenges for FinFETs has been that strong localization of the wavefunction along the fin has made sufficient tunability of the exchange interaction challenging. We show that exchange can be tuned both by adjusting the detuning between gates P1 and P2 or with the voltage applied to the central barrier gate (B) which tunes the tunnel coupling and thus exchange symmetrically. The range of tunability ranges over at least two orders of magnitude reaching values of J/h larger than 200 MHz.

III. Outlook

The next goal is to extend the single and two-qubit gates to a chain of qubits along a fin and to show that this can be realized reproducibly. Then scalable initialization, read-out and coupling of multiple 1D qubit chains will be a next big goal on the path towards realizing a 2D network [16,17] of coupled silicon-based spin qubits as required for the implementation of error correction (see Fig. 7).

Acknowledgment

We thank the Cleanroom Operations Team of the Binnig and Rohrer Nanotechnology Center (BRNC) for their help and support. This work was partially supported by the Swiss National Science Foundation through NCCR SPIN (grant no. 51NF40-180604). It has additionally received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Sklodowska-Curie grant agreement No. 899018 and the COFUND Action QUSTEC under grant agreement No. 847471.

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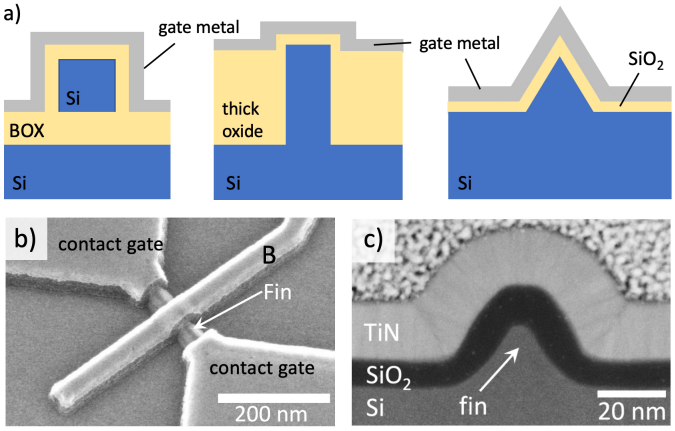

Fig. 1. a) Schematic representation of three FinFET technologies used for the definition of spin qubits. b) Scanning electron microscope (SEM) image of the first gate-layer of a single gate (B) device. The two contacts are covered with contact gates to accumulate source and drain regions. c) Transmission electron microscope (TEM) image of the triangular fin cross-section. Dots are accumulated near the apex of the fin.

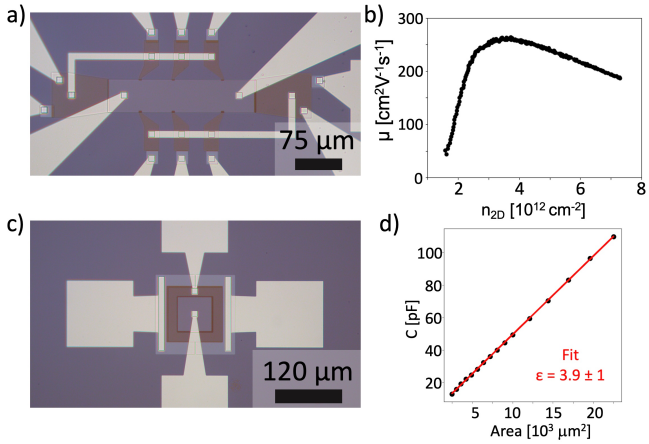

Fig. 2. a) Hall bar test device that allows separate accumulation of the contact regions and the channel with individual gates. b) Example density vs. mobility plot for holes as extracted using Hall measurements. c) Capacitance vs. voltage test device with separate tunability of the circular contact region such as to separate contact resistance from channel effects. d) Dielectric constant extracted from a fit of the capacitance to the channel area of devices with different size.

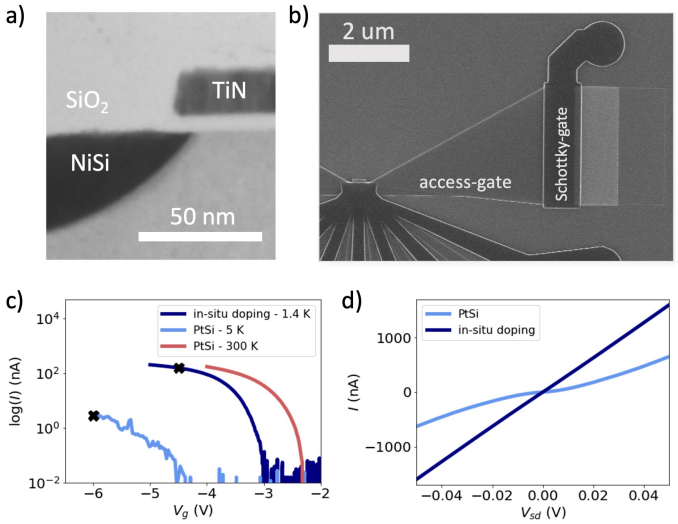

Fig. 3. Contact resistance: a) TEM image of the contact to gate interface for an ambipolar NiSi FinFET device. b) SEM image of a FinFET device with separate access- and Schottky-gate. c) Current vs. gate voltage V_g of two large channel transistor devices with PtSi and in-situ doped contacts at various measurement temperatures and for a fixed source-drain bias of 5 mV. d) Current vs. source-drain bias for these devices at the gate voltages indicated by the crosses in c), i.e. at similar overdrive voltages.

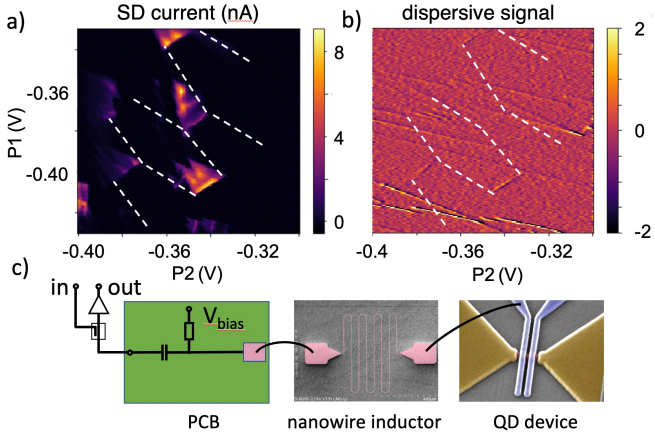

Fig. 4. a) Measurement of source drain current through a single gate-layer double quantum dot with bias triangles showing up at triple points. b) Reflectometry from a tank circuit at 482 MHz connected to the plunger gate P1 showing interdot transitions and background of transitions to unintentionally confined states. c) Schematic (left) of the tank circuit with a superconducting inductor on a separate chip (SEM image, middle) and (right) SEM image of a device similar to the one that was measured.

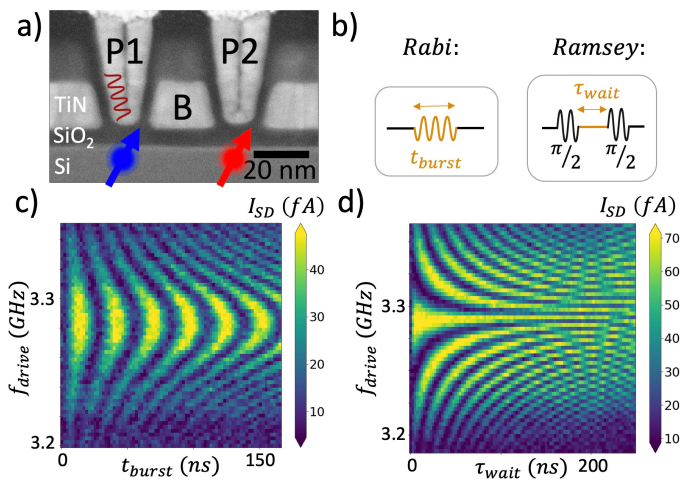

Fig. 5. a) TEM cross-section of the gates in a double quantum dot device with two holes accumulated below the second gate-layer gates P1 and P2. b) Pulse sequences used for Rabi and Ramsey experiments as applied to gate P1 in a). c) Measured Chevron pattern resulting from Rabi driving as a function of frequency and pulse duration at a temperature of T = 1.4K. The observed oscillations occur at a Rabi frequency of f_{Rabi} = 36 MHz with T_2^{Rabi} > 800 ns. d) Ramsey experiment at the same temperature resulting in a T_2^* = 280 ns.

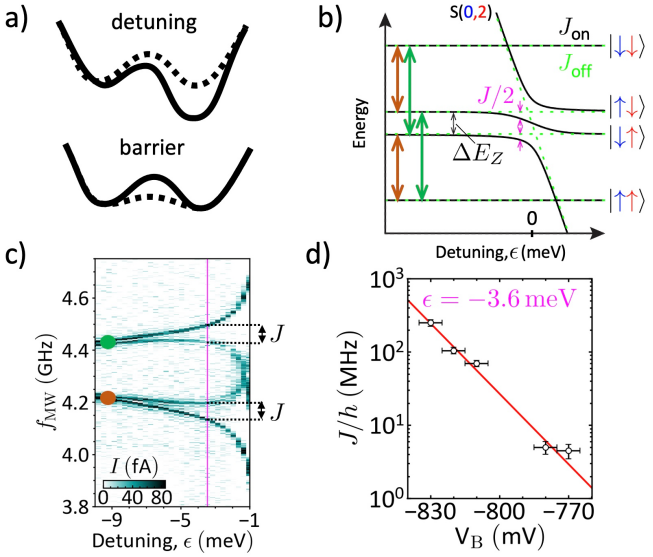

Fig. 6. a) Exchange can be tuned either by detuning the energy of the two dots or by lowering the central potential barrier. b) Energy levels of the double dot near the symmetric (ε = 0) point where exchange is strongest. For large detuning the energy difference between $|\uparrow,\downarrow>$ and $|\downarrow,\uparrow>$ is given by the difference in g-factor between the two hole spins. c) Spectroscopy showing the S(0,2) contribution after applying a microwave pulse and adiabatically moving to positive detuning. The red and blue dots correspond to the transitions indicated by the arrows in b). d) Measurement of J/h at fixed detuning (ε = -3.6 meV) when varying the potential barrier between the dots with the barrier gate voltage V_B .

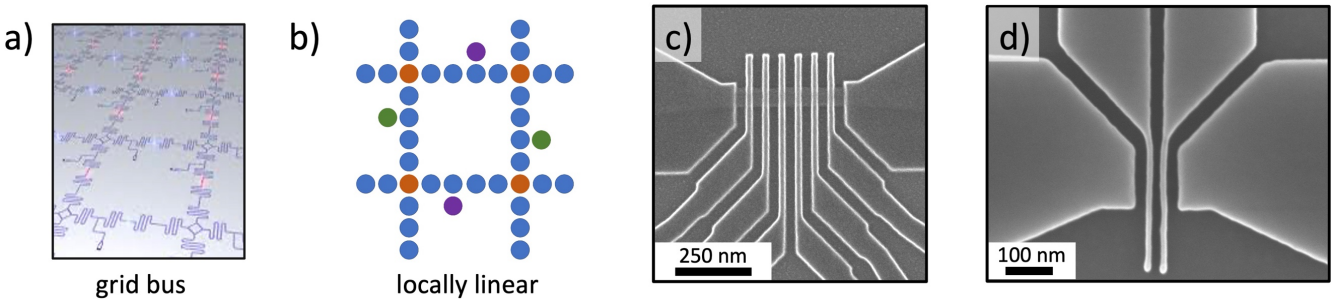

Fig. 7. Towards 2D arrays: Coupling between hole spins in FinFETs can be realized e.g. a) with resonators or b) with exchange and shuttling between neighboring qubits. In this second, locally linear architecture, shuttling or swaps are used to propagate quantum states and junction elements (brown), scalable read-out (purple) and loading (green) are required. c) SEM image of an exemplary structure for a linear chain of qubits. d) SEM image of test structure for improved lithographic resolution which may help overcome residual disorder through additional tunability. Here the pitch of the first gate layer gates is 30 nm.