QUANTUM HARDWARE

Transistor qubits heat up

Hole spin qubits that operate at temperatures close to 4 K can be created in fin field-effect transistors similar to those used in advanced integrated circuits.

Romain Maurand and Xavier Jehl

Seventy five years after its invention, the transistor is ubiquitous in electronics, and the deterministic channel conductance modulation in field-effect transistors (FETs) controls the operation and behaviour of entire integrated circuits. This classical working principle is, however, in contrast to that of a quantum circuit. The building block of a quantum processor is a two-level system — a quantum bit or qubit — that lives as a superposition of 0 and 1. The outcome of a quantum circuit is statistical (we will know the probability of being in a certain state) and quantum bits can be encoded in various physical supports including photons, ions and superconducting circuits.

Over the past ten years, silicon has been established as a platform for quantum computation with qubits based on single electronic spins isolated in multi-gate devices. This has brought hope that the silicon-scaling capabilities developed for microelectronics might help accelerate the development of large-scale silicon quantum processors. However, the potential of transistors to make high-quality qubits remains uncertain. Writing in *Nature Electronics*, Dominik Zumbühl, Andreas Kuhlmann and colleagues now report the development of a fully functional spin qubit in a FinFET transistor structure similar to those used in today's microelectronic integrated circuits[1].

Beyond the usual figures of merit for qubits such as coherence or manipulation speed, the researchers — who are based at the University of Basel and IBM-Research in Zurich — examined the high-temperature operation of the devices. This is crucial, as the best silicon spin qubit figures of merit are typically reported at vanishingly low temperatures: below 0.1 K for silicon metal–oxide–semiconductor (MOS) systems[2] and silicon/silicon germanium heterostructures[3]. At these temperatures, the available cooling power is extremely small, limiting the ability of operating large quantum circuits integrated with dissipative classical control electronics[4]. Kuhlmann and colleagues instead demonstrate spin qubit functionality above 4 K, where cryogenic constraints are much less stringent.

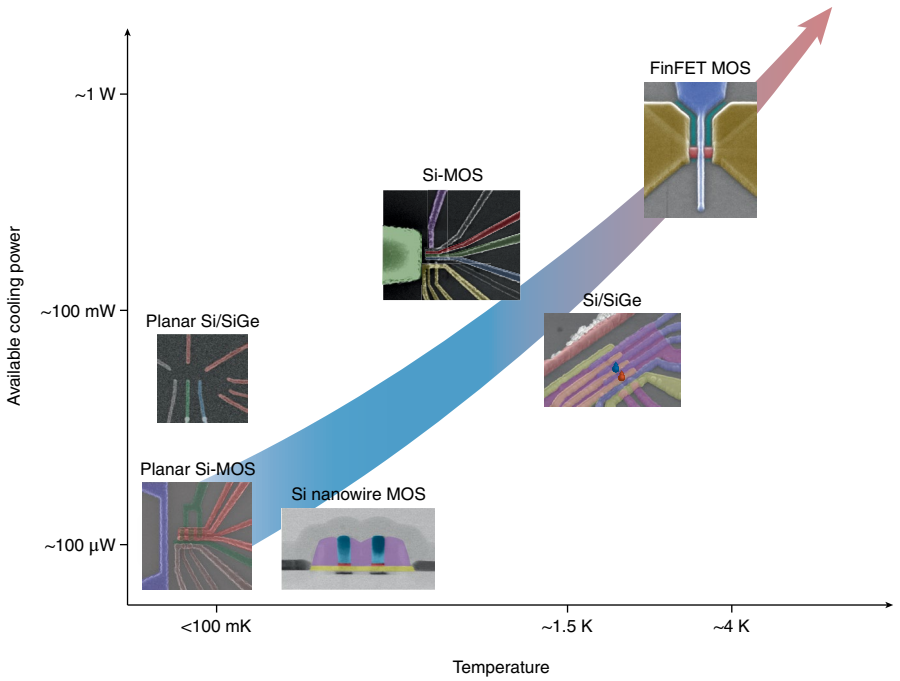

Fig. 1 | Silicon spin qubit platforms and their operating temperatures. The graph highlights experiments that have demonstrated quantum logic with spin qubits in silicon, plotted against their operating temperature and corresponding available cooling power. The best qubit figures of merit have been reported for experiments below 100 mK in silicon spin qubit platforms: planar Si-MOS (ref. [2]), planar Si/SiGe (ref. [3]) and Si nanowire MOS (ref. [5]). At those temperatures, the available cooling power is too small to be able to integrate dissipative control electronics with the quantum chip. Reports for Si-MOS (ref. [6]) and Si/SiGe quantum logic above 1 K (ref. [7]) indicate that silicon quantum processors can be operated in pumped ^{4}He systems with milliwatt-level cooling power, enabling future integration with dissipative control electronics. The work of Kuhlmann and colleagues[1] provides a new silicon hole spin qubit platform that is based on FinFETs and has operating temperatures close to 4 K. Images reproduced with permission from: planar Si-MOS, ref. [2], Springer Nature Ltd; planar Si/SiGe, ref. [3], Springer Nature Ltd; Si nanowire MOS, ref. [5], under a Creative Commons licence (CC BY 4.0); Si-MOS, ref. [6], Springer Nature Ltd; Si/SiGe, ref. [7], Springer Nature Ltd; FinFET MOS, ref. [1], Springer Nature Ltd.

In order to turn transistors into qubits, the role of the channel has to be reassessed. A classical transistor needs a unique gate on top of the channel, but a quantum transistor has to have short gates (less than 40 nm) with a pitch well below 100 nm to turn the channel into a linear chain of quantum dots and create isolated single electrons or holes below each gate. The researchers achieve this with a silicon fin-shaped channel using complementary metal–oxide–semiconductor (CMOS) fabrication techniques and a self-aligned second gate layer, leading to a dot size of around 7 nm.

Working with a p-MOS double quantum dot, the researchers isolate two hole spins in a FinFET. By measuring the channel current, the two spin qubit

states are inferred using Pauli spin blockade spin-to-charge conversion. The electron spin degree of freedom is typically manipulated with high-frequency magnetic fields (such as in conventional nuclear magnetic resonance). But, with holes, the spin qubit can couple directly to high-frequency electric fields thanks to the characteristics of the valence band of silicon, which exhibits spin–orbit coupling. By applying microwave pulses to the gate, the researchers can coherently control and characterize their hole spin qubit up to a temperature of 4 K. Notably, even at 1.5 K they were able to demonstrate single-qubit gate fidelities at the fault-tolerant threshold with ultrafast qubit driving.

Today, cooling down to 3.5 K requires only thermal machines based on pulse tubes, which offer more than a watt of cooling power. It is also possible using a liquid helium bath, and pumping over such a bath allows temperatures of around 1.5 K to be reached with reasonable additional complexity. There is though a gap if one needs to reach temperatures well below 1 K. It requires a complex closed-circuit circulation involving helium-3, a rare isotope of helium produced from nuclear warheads, which also brings geopolitical challenges. However, for more than a decade, the availability of cryogen-free dilution refrigerators has helped the rapid development of spin and superconducting qubits. While they are now very reliable and easy to use, these expensive setups offer a limited cooling power on the order of 0.5 mW at 0.1 K. A key motivation for operating silicon spin qubits above 1 K is thus the availability of simpler cryogenic apparatus with larger cooling powers and the potential scalability it brings (Fig. 1).

The qubit readout technique used by Kuhlmann and colleagues is too slow to provide the single-shot readout needed for future applications, but it could be replaced with faster readout approaches that use reflectometry techniques. However, reaching high-fidelity readout at high temperatures remains challenging. Another issue is control over the size of the quantum dots and their location inside the FinFET channel. The inferred dot size here is markedly smaller than any critical dimension that can be well controlled by lithography. Hence, there is a large dispersion between devices, which will have to be addressed for future scaled-up architectures. ❐

Romain Maurand ✉ and Xavier Jehl ✉
CEA-Grenoble, Université Grenoble Alpes and Grenoble-INP, PHELIQS laboratory, Grenoble, France.
✉*e-mail: romain.maurand@cea.fr; xavier.jehl@cea.fr*

Published online: 18 March 2022
https://doi.org/10.1038/s41928-022-00736-8

References
1. Camenzind, L. C. et al. *Nat. Electron.* https://doi.org/10.1038/s41928-022-00722-0 (2022).
2. Veldhorst, M. et al. *Nat. Nanotechnol.* **9**, 981–985 (2014).
3. Yoneda, J. et al. *Nat. Nanotechnol.* **13**, 102–106 (2018).
4. Xue, X. et al. *Nature* **593**, 205–210 (2021).
5. Maurand, R. et al. *Nat. Commun.* **7**, 13575 (2016).
6. Yang, C. H. et al. *Nature* **580**, 350–354 (2020).
7. Petit, L. et al. *Nature* **580**, 355–359 (2020).

Competing interests
The authors declare no competing interests.