SPIN Journal Club 19-09-2022, arXiv:2208.12131

Scalable on-chip multiplexing of low-noise silicon electron and hole quantum dots

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PhD thesis (12/2018):
Cryogenic electronics and quantum dots on silicon-on-insulator for quantum computing

supervised by Marc Sanquer (Grenoble)

Previous work by VTT and John Morton's group

Applied Physics Letters ARTICLE scitation.org/journal/apl

Dispersive readout of reconfigurable ambipolar quantum dots in a silicon-on-insulator nanowire

Cite as: Appl. Phys. Lett. **118**, 164002 (2021); doi: 10.1063/5.0040259
Submitted: 11 December 2020 · Accepted: 9 March 2021 ·
Published Online: 20 April 2021

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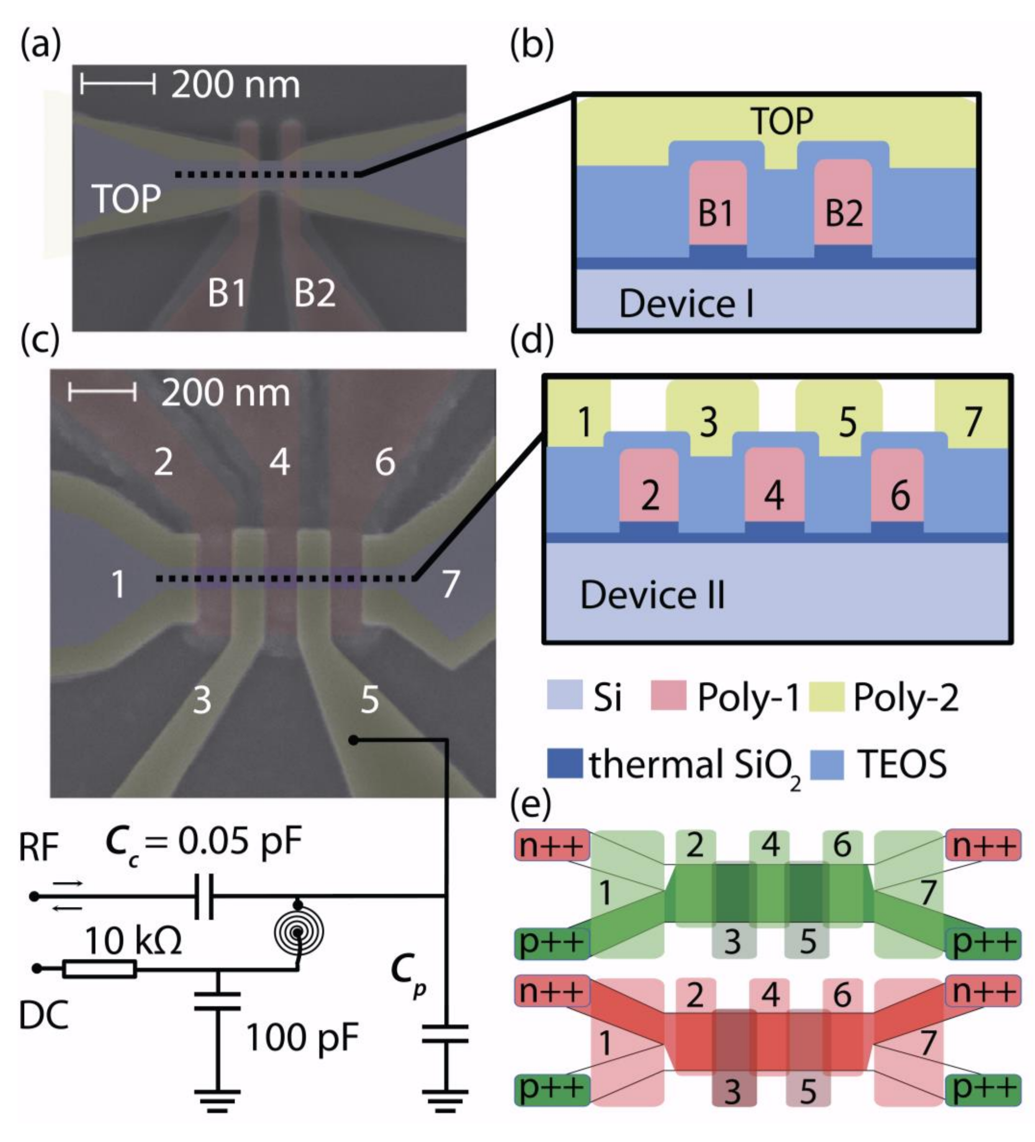
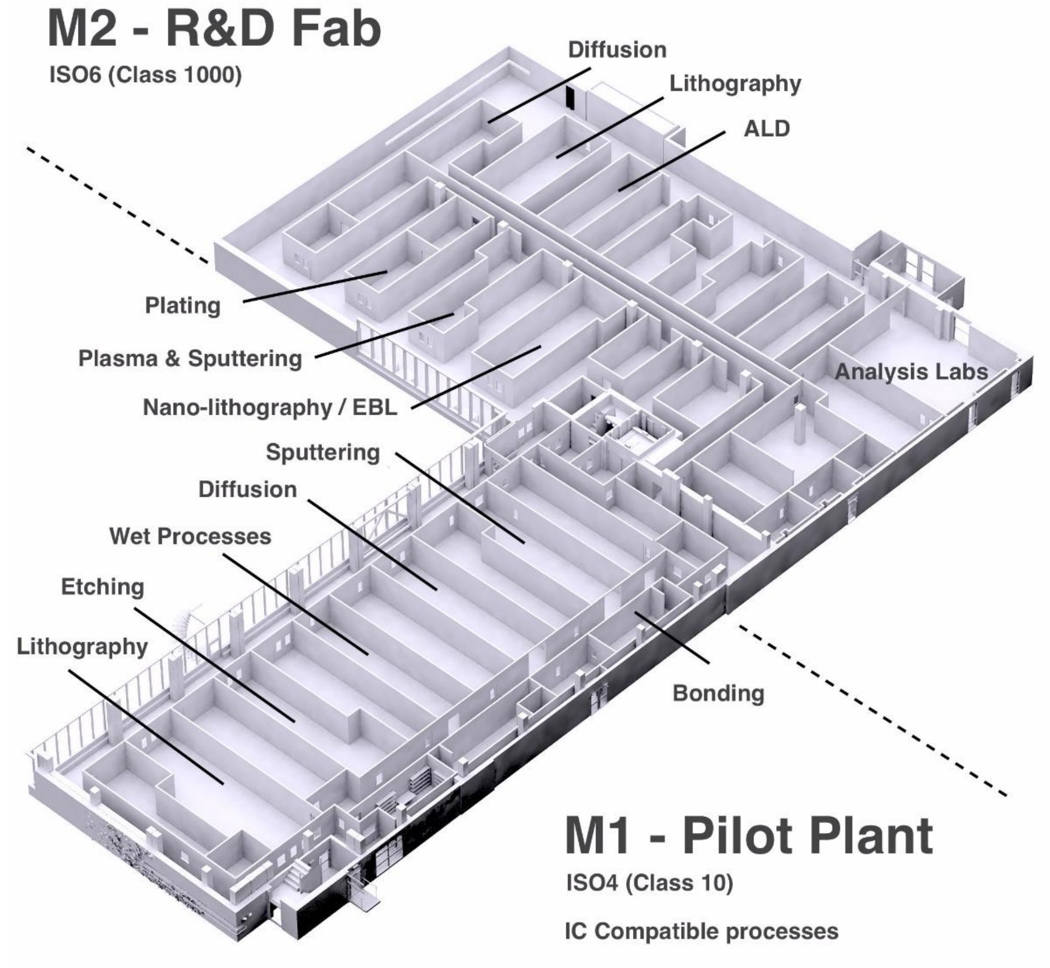
Previous work by VTT and John Morton's group



Duan *et al.*, APL **118**, 164002 (2021)

VTT's Micronova cleanroom facilities

Based in Espoo, Finland; jointly run by VTT and Aalto University; total area of 2600 m^2



https://www.vttresearch.com/en/ourservices/micronova-center-applied-micro-and-nanotechnology

Processing capabilities in Micronova fab: VTT has more than 200 equipment in the semiconductor fab.

Lithography

- i-line stepper, 5:1, 0.35 µm CD
- Contact/proximity aligners
- Electron-beam writing
- Nanoimprinting (step & stamp)

Etching

- Polysilicon/nitride
- Oxide; thin film and Advanced Oxide Etching
- Metals; Al, Mo, Ti-W, Nb (TCP)
- Deep silicon etching;
- Anhydrous HF vapor
- Wet etching, various
- Critical-point drying

Deposition

- Six sputtering tools
- LPCVD of nitride, poly, and oxide
- TEOS, LTO
- PECVD; nitride and oxide
- ALD: aluminium oxide, titanium oxide
- Parylene

Plating, Spin Coating

- Cu (via or wiring), Ni, Sn-Ag, Sn-Pb,
- In-Sn, Au
- Polyimide, BCB

3D Integration

- CMP of Si/oxide or copper
- Direct wafer bonding
- Grinding
- Spin-etching
- Thin-wafer handling
- Ion trimming

Characterization

- Scanning electron microscope
- Scanning probe microscope
- Scanning acoustic microscope
- Optical film characterization
- Profilometers
- Atomic force microscope
- Alignment accuracy measurement
- Wafer defect inspection system

Back End

- Wafer dicing
- Flip-chip bonding
- Wire bonding
- Thermal compression bonding

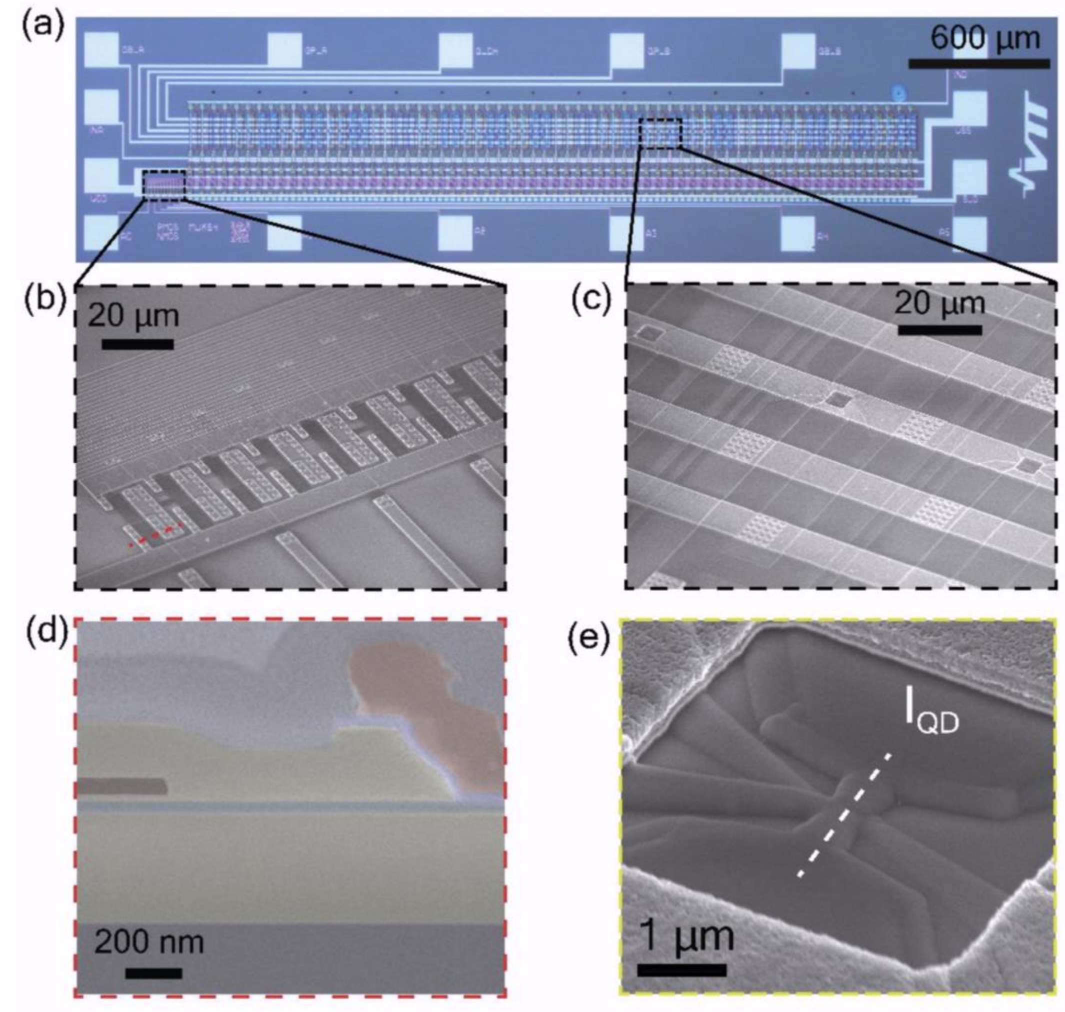
Ion Implantation

- Medium-current; n- or p-type doping of silicon

Testing

- Wafer level test systems
- High speed electrical and optical testing capabilities
- Multiple labs for offline testing and characterization

Key findings



Scalable on-chip multiplexing of low-noise silicon electron and hole quantum dots

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- Hybrid quantum-dot-CMOS technology:
  - QDs embedded in a 64-channel **cryogenic CMOS multiplexer**
  - scalable interfacing of up to millions of QDs for variability analysis and qubit geometry optimization
- Low-noise electron and hole QDs:
  - unprecedentedly low charge noise at 5.6K
  - CMOS process that utilizes a conventional **doped-Poly-Si/SiO2/Si MOS stack**

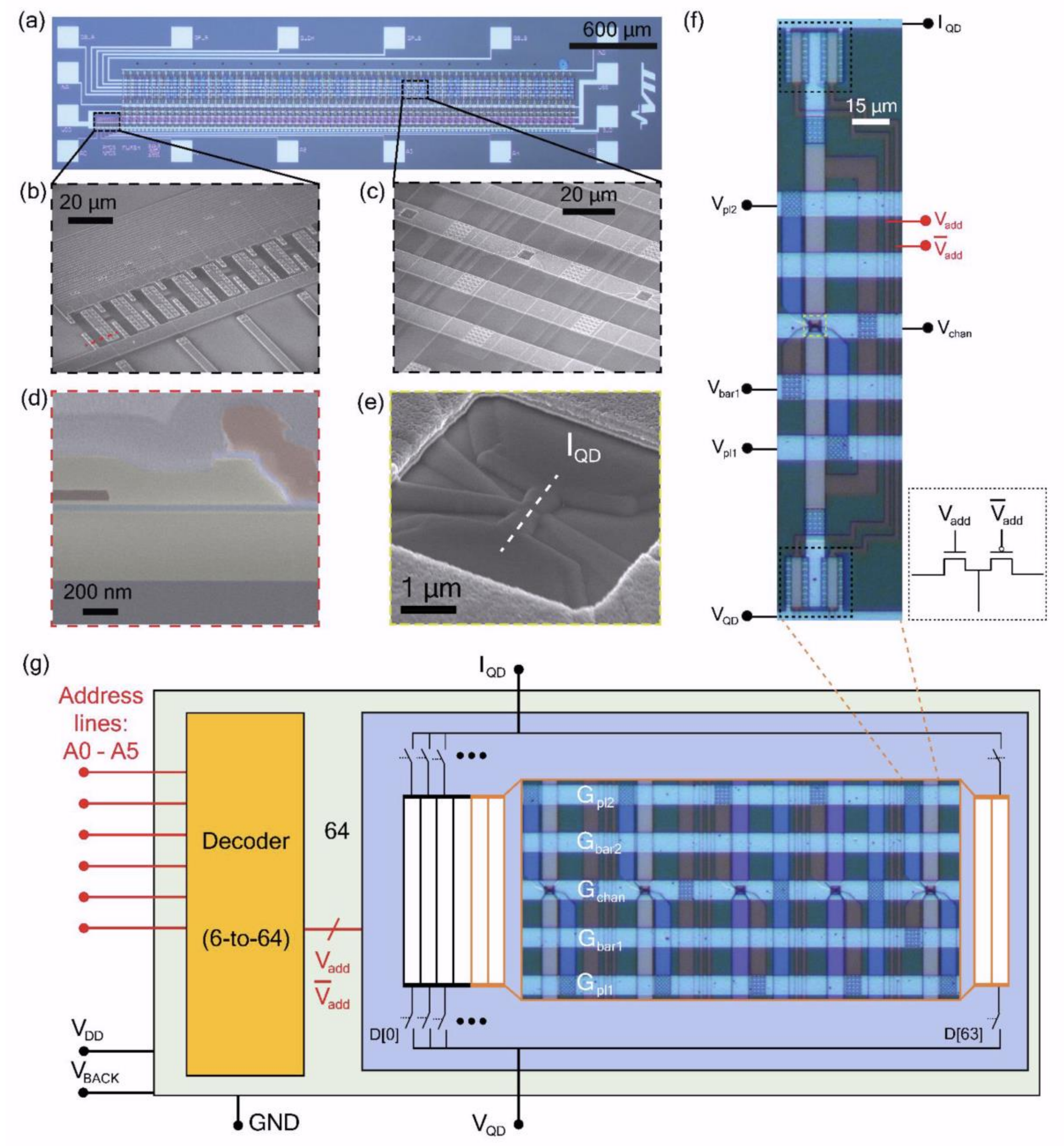
Device fabrication

- 150mm silicon-on-insulator wafers (t_{BOX}=400nm)
- 8 UV and 3 e-beam lithography layers
- Gate oxide: **20nm thermal SiO_2**
- **NW (fin) height = 24nm, NW width = 70nm**
- n++ doped Poly-Si (thickness = 50nm (1st gate layer)/ 80nm (2nd gate layer)
- RT resistivities of Poly-1 and Poly-2 films: $1.14\mathrm{x}10^{-2}$ Ωcm and $0.19\mathrm{x}10^{-2}$ Ωcm
- **Gate length 50nm, gate pitch 100nm (?)**
- **Gate layer isolation oxide: 35nm LPCVD SiO_2**
- Ohmic contacts: phosphorous (n-type) or boron (p-type) implantation
  - 250nm LPCVD SiO_2, anneal at 950C to activate dopants and anneal the dielectrics
- Contact holes for all three layers
  - dry and wet etching processes
  - metallization layer consisting of 25nm TiW and 250 nm AlSi
- Forming gas anneal

Mobilities from [1]: $\mu_e = 608$ $\mathrm{cm^2/Vs}$, $\mu_h = 260$ $\mathrm{cm^2/Vs}$

[1] Duan *et al.*, APL **118**, 164002 (2021)

Multiplexer, CMOS logic and quantum dots



- Cryo-MUX consists of a 6-to-64 decoder and analog switches (pairs of n- and p-MOSFETs)
- To select one of the devices (24 electron and hole single QDs, 24 e and h DQDs, 16 test NWs) a combination of the A0-A5 voltages is supplied to the decoder
- To have the switch transistors fully open V_{add}=1.5V is applied
- All 64 devices share the same 5 chip terminals to drive the gate voltages
- Cryo-CMOS logic leakage current <1pA, corresponding to the sub-pW power dissipation level

Subthreshold swing

su

T-

SS

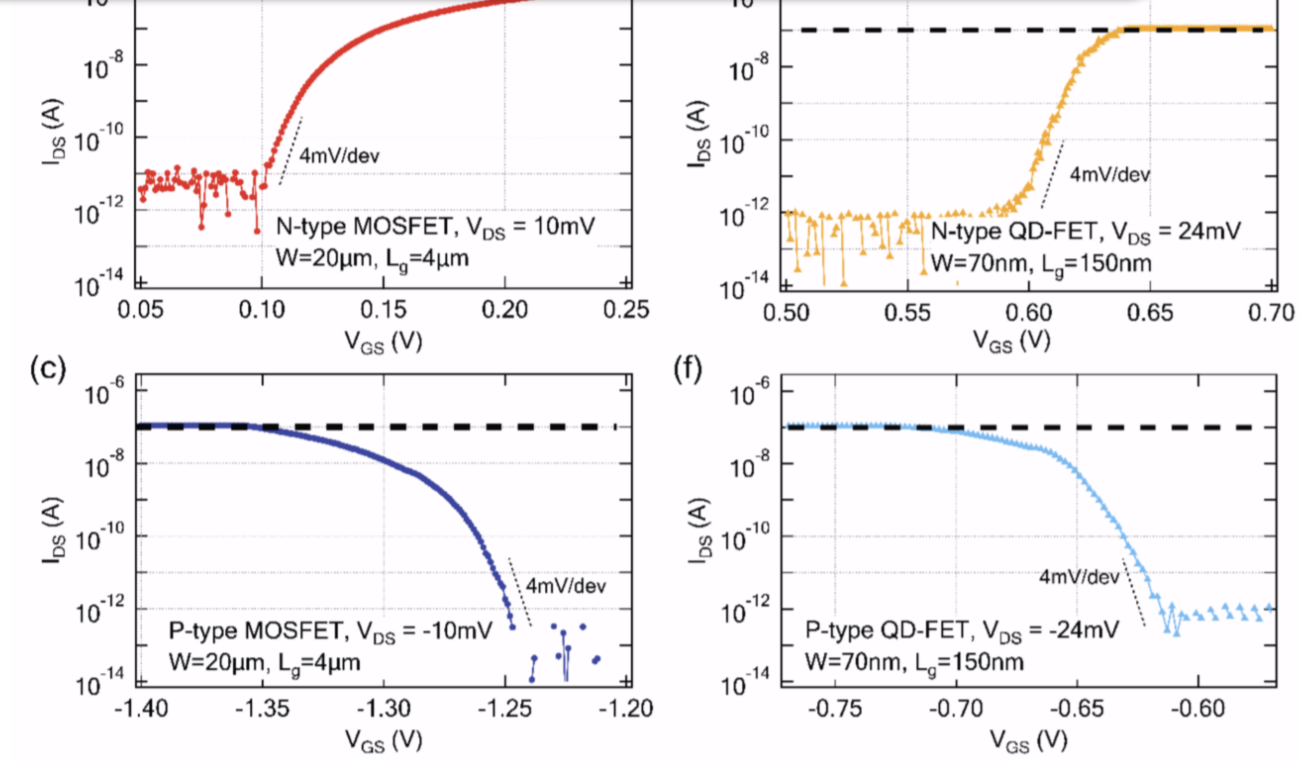
Low disorder due to **Poly-Si/SiO_2/Si process** and not:
*"The recently demonstrated **foundry-grade** hole and electron spin qubits used the advanced fabrication process with a high-k metal gate (HKMG) with either high-k oxide and metal gate [9,11] or just a metal gate in the gate stack [10, Basel-IBM devices]*

Assuming linear T-scaling: 80mV/dec/300K*5.6=1.5mV/dec

$SS(5.6K)$ =4 mV/dec

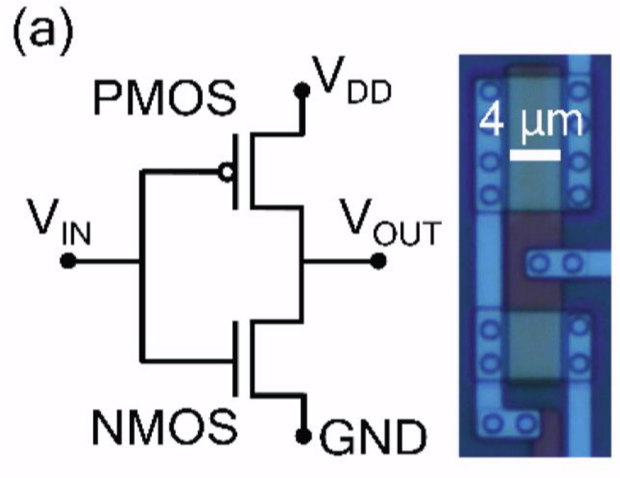
SS-saturation due to a **disorder-induced** tail in the DOS below the edge of conduction and valence bands

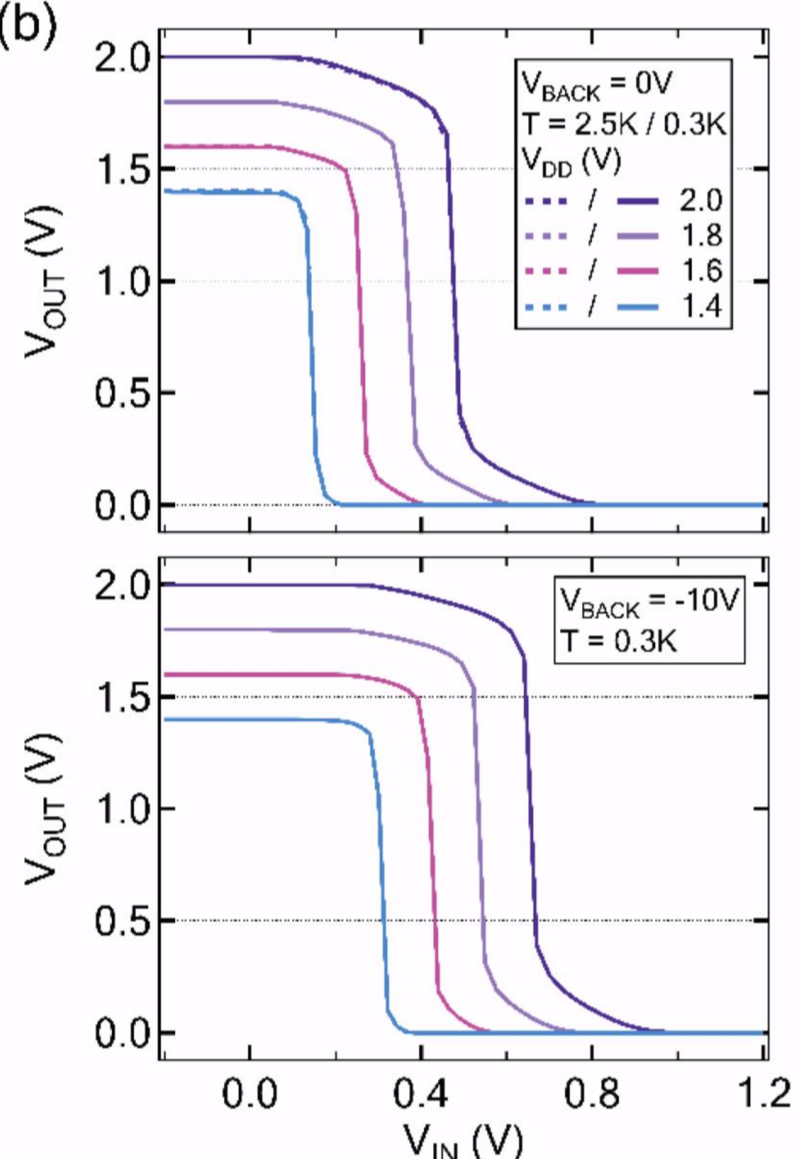
4 mV/dec is the world's sharpest to-date SS values of 4 mV/dec
(4 mV/dec value corresponds to 1.5meV band tails below E_c and E_v)

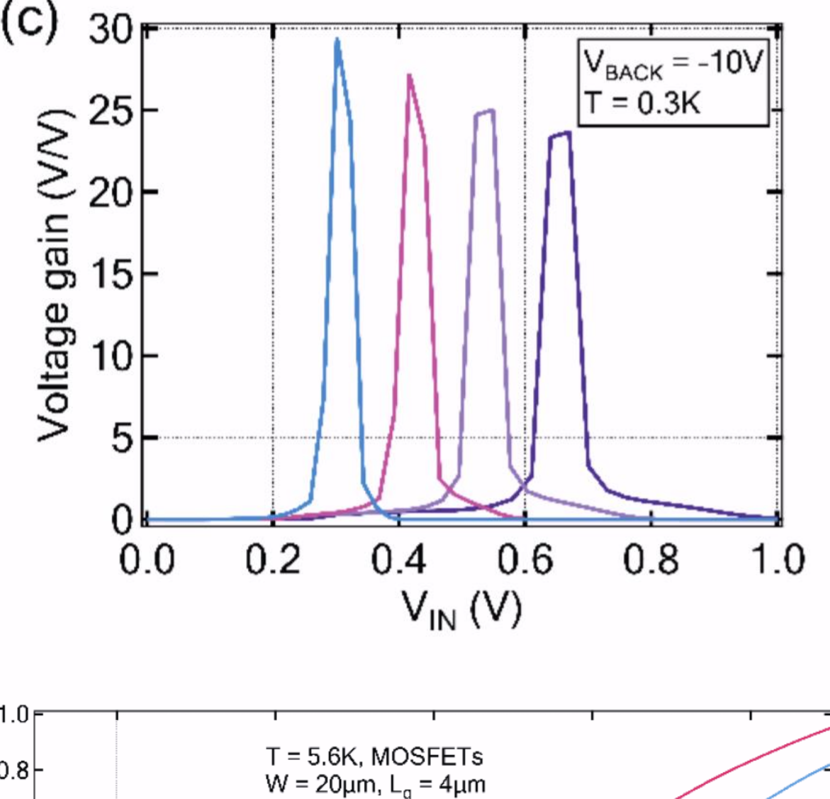


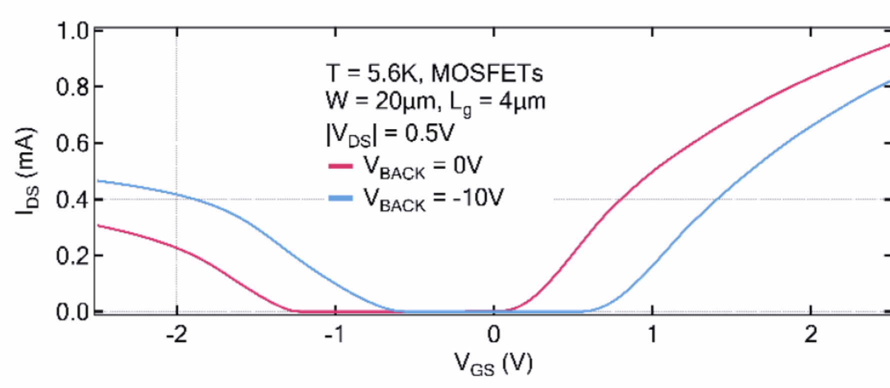
Bohuslavskyi et al., IEEE Electron Device Letters 40, 5, 784 (2019)

CMOS inverter



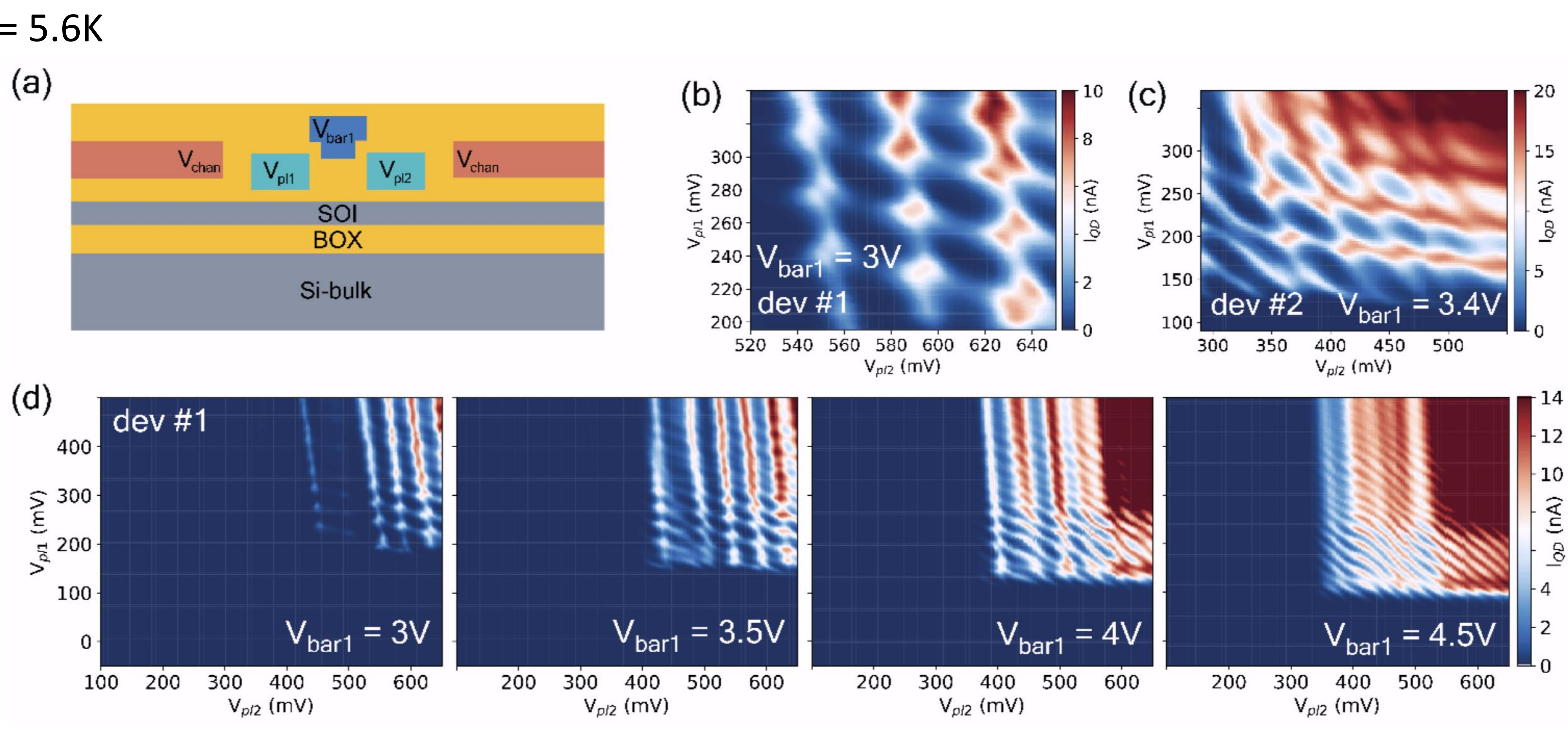






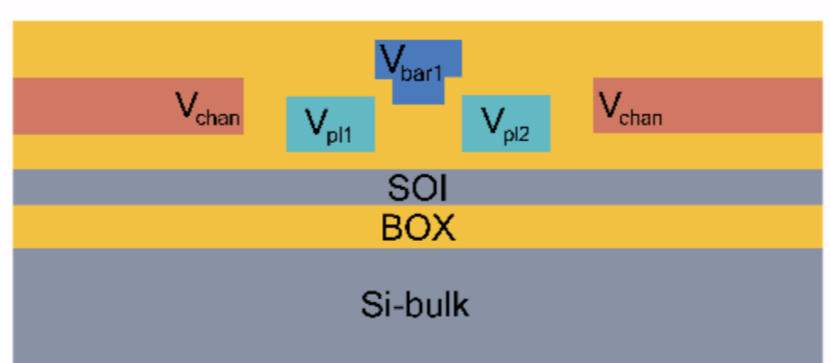
Tunable few-electron double quantum dots

T = 5.6K

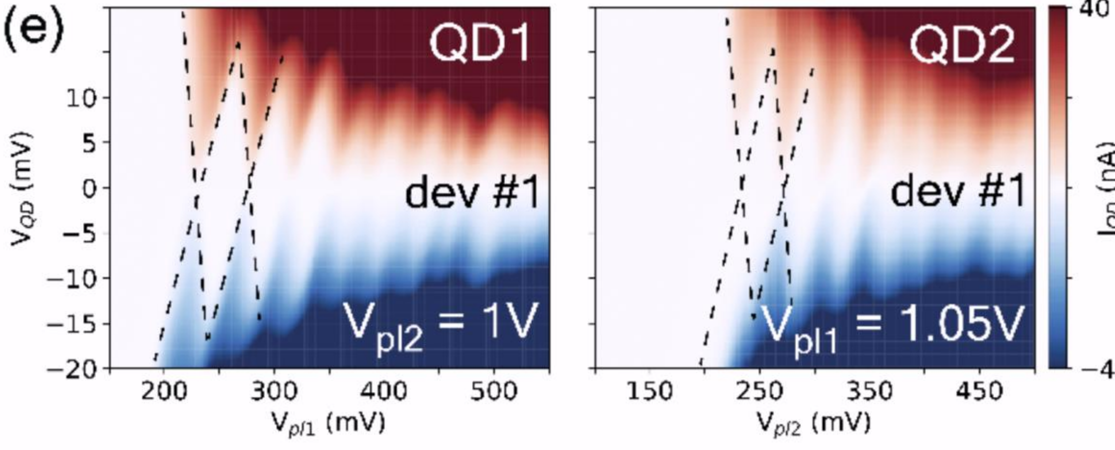


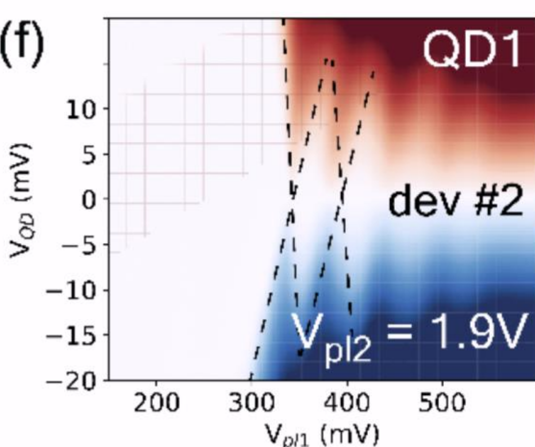
Tunable low-noise electron and hole QDs

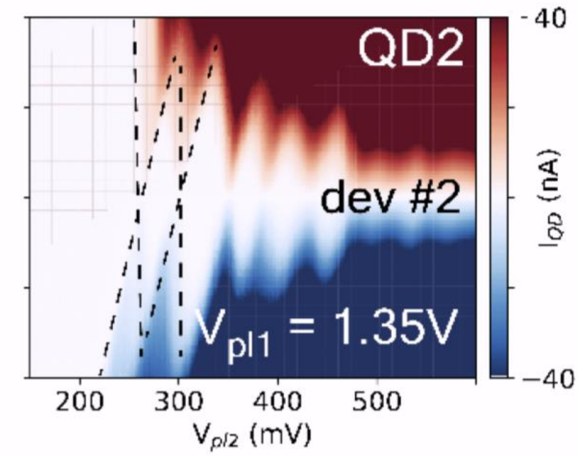
T = 5.6K



Current devices have **no charge sensor**
→ dc transport measurements: they assume that the few-electron/hole regime has been reached







Low-frequency charge noise in electron QDs

(a) dev#1, QD1
sweeping up
sweeping down
I_{qd} (nA)
V_{pl1} (V)

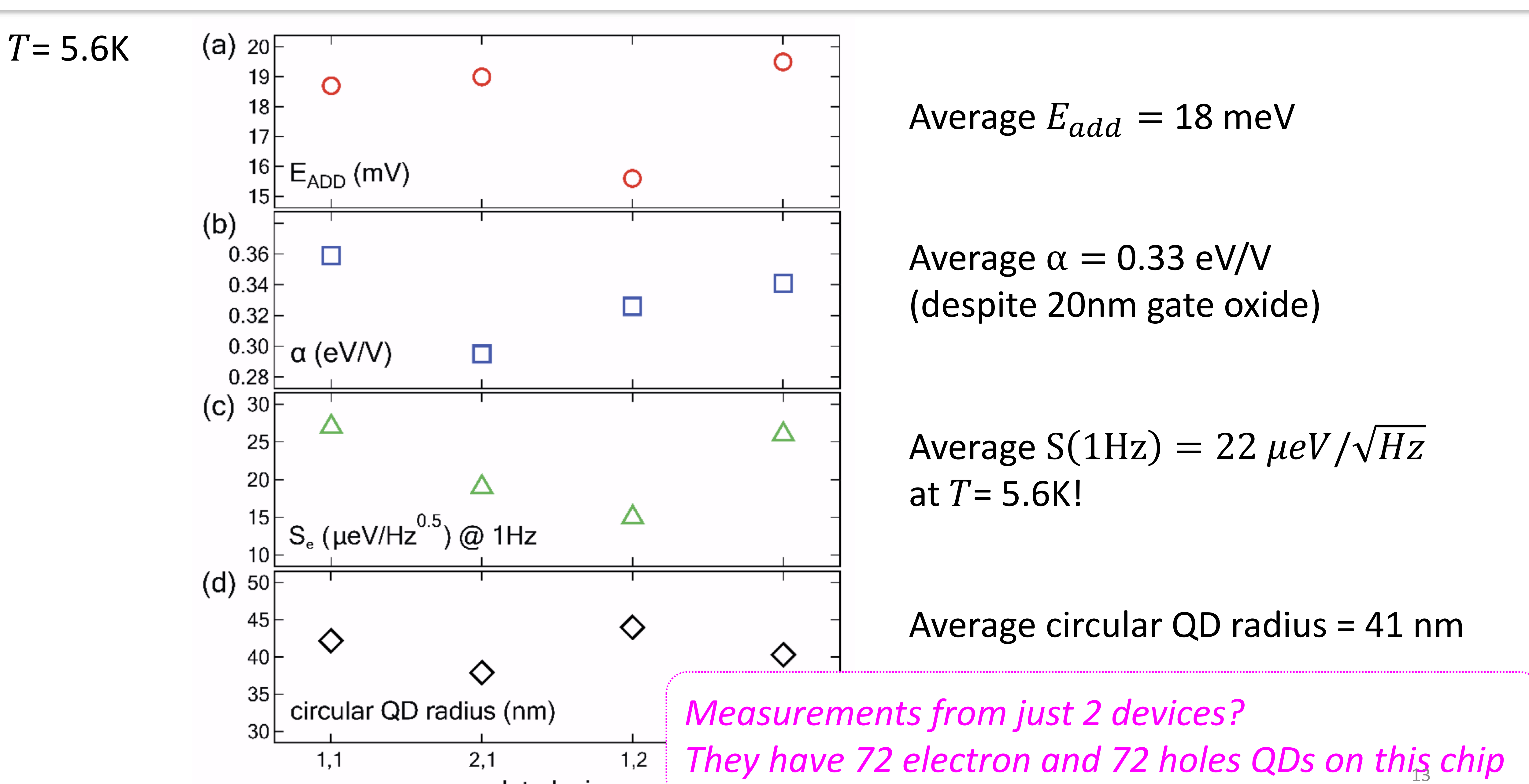
(b) dev#1, QD1
g_{m-pl1} (nS)
V_{pl1} (V)

(c)
background
1/f slope
1st, top
1st, left
1st, right
2nd, left
2nd, right
3rd, left
3rd, right
S_I (A^2/Hz)
f (Hz)

(d) dev#1, QD1
S_e ($\mu eV/Hz^{0.5}$)
f (Hz)

(e) dev#1, QD1
(f) dev#2, QD1
(g) dev#2, QD2
1st, left
1st, right
S_e ($\mu eV/Hz^{0.5}$)
f (Hz)

Quantum dot variability



Charge noise at 1 Hz

This work:
average $S_e(1\text{Hz}) = 22\ \mu eV/\sqrt{Hz}$
average $S_h(1\text{Hz}) = 28\ \mu eV/\sqrt{Hz}$
at T= 5.6K in the few-electron/hole regime(?)

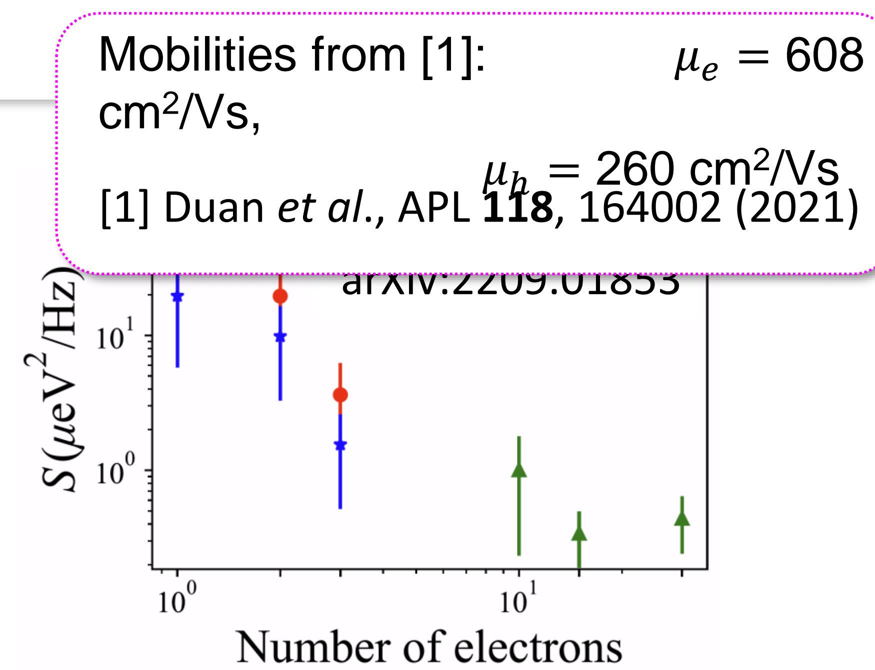
Assuming linear T-scaling of charge noise:
Estimated charge noise at 100 mK: $\simeq 0.4\ \mu eV/\sqrt{Hz}$

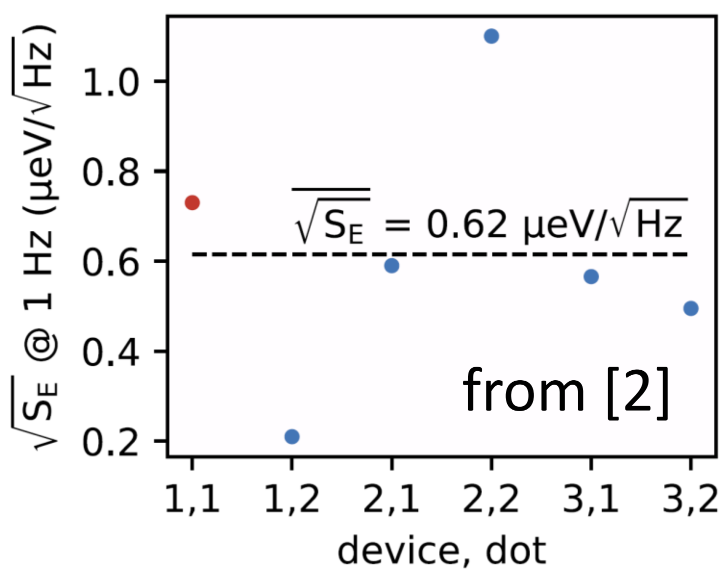
Lowest noise values reported so far for
Ge/SiGe heterostructure QDs: $0.62\ \mu eV/\sqrt{Hz}$

Reason for low-disorder:
all-silicon gate-stack (IMEC $3.6\ \mu eV/\sqrt{Hz}$)

Mobilities from [1]: $\mu_e = 608$ cm²/Vs, $\mu_h = 260$ cm²/Vs

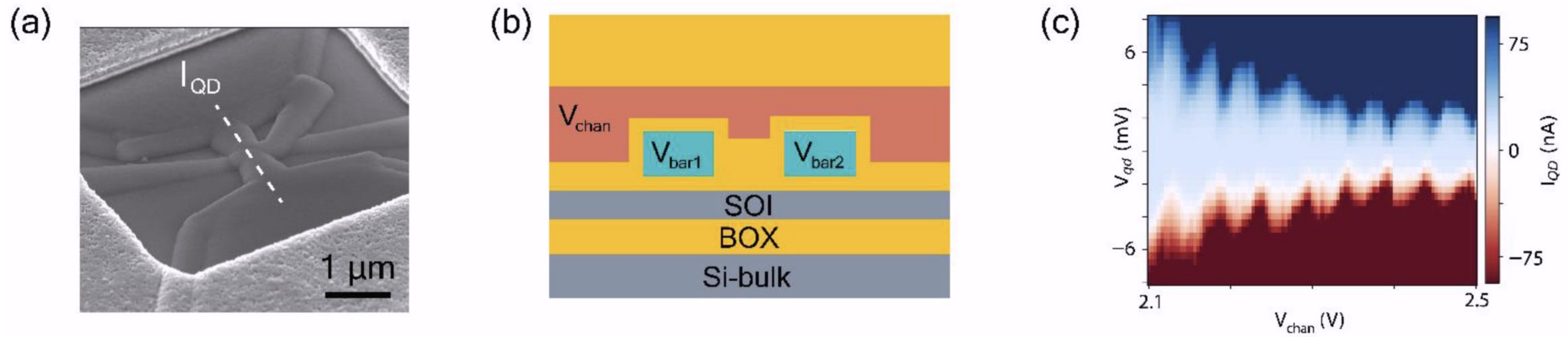
[1] Duan *et al.*, APL **118**, 164002 (2021)





[1] Petit et al., PRL **121**, 076801 (2018), [2] Lodari *et al.*, Mater. Quantum. Technol. **1,** 011002 (2021)

Electron QDs at 300mK



Extended data Fig. 7 | Electron quantum dots at 300 mK. (a) A tilted SEM image of the test device measured in a simpler 8-channel MUX with the same circuit topology for the decoder and switches as in 64-channel MUXes #1 and #2 discussed in the main text. **(b)** The cross-section schematic of the device (a). **(c)** Coarse-resolution stability diagram showing Coulomb diamonds of the test device measured at 300 mK. Both, quantum dot devices and cryo-CMOS function at sub-Kelvin temperatures.