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Letter

A Flexible Design Platform for Si/SiGe Exchange-Only Qubits with Low Disorder

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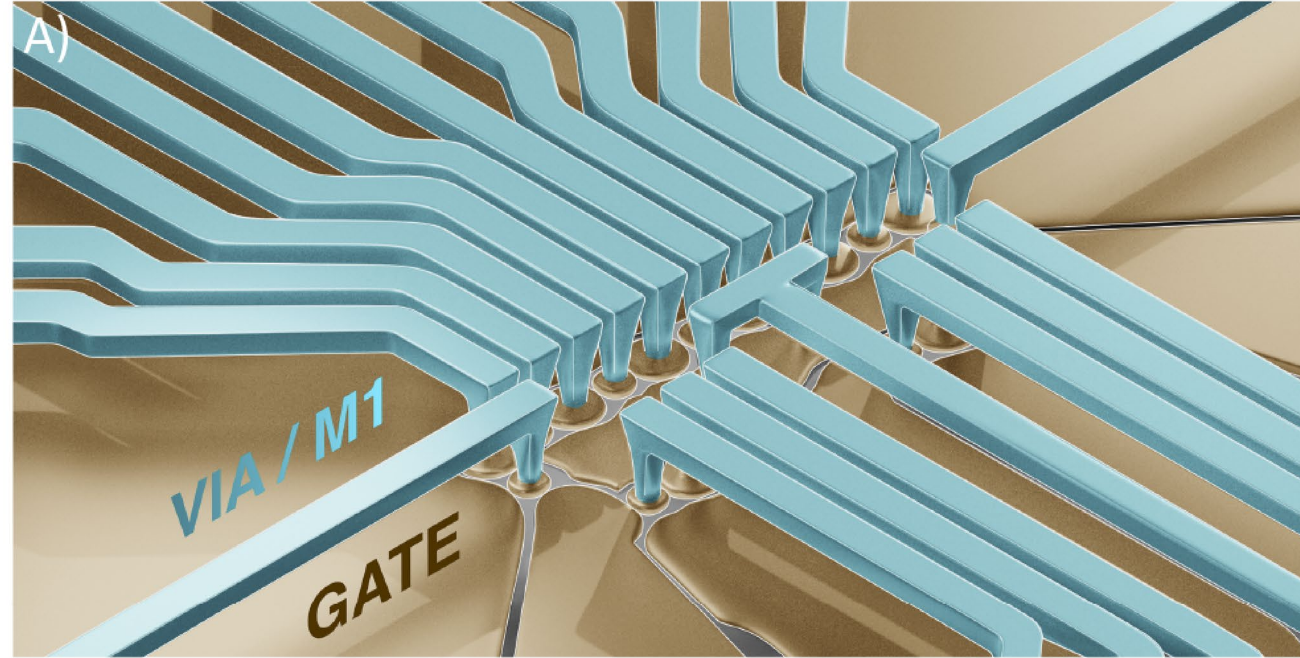
SLEDGE (single-layer etch-defined gate electrodes)

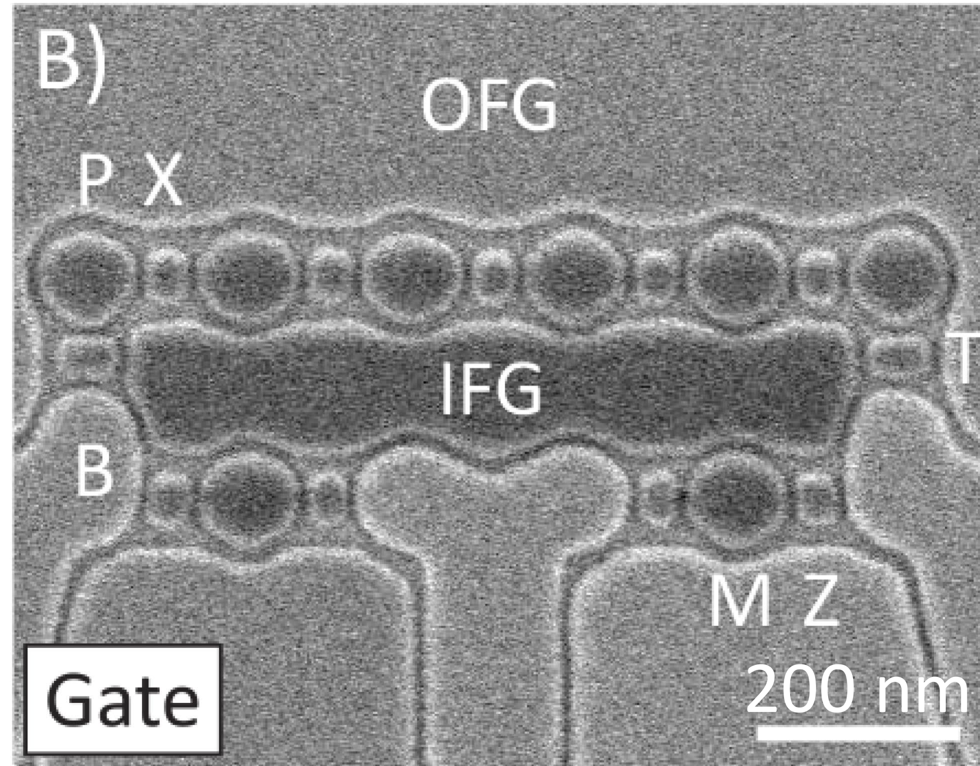


A SLEDGE device consists of

1) a gate layer (“M0”), in which all gates are patterned simultaneously on the same plane → uniplanar gate arrangement
2) back-end-of-line (BEOL) interconnect layers, in which vertical vias contact gates and then spans (“M1”) connect vias to macroscopic routing

Gate-level design

SLEDGE devices designed for triple-dot exchange-only qubit operation



Key features of SLEDGE:

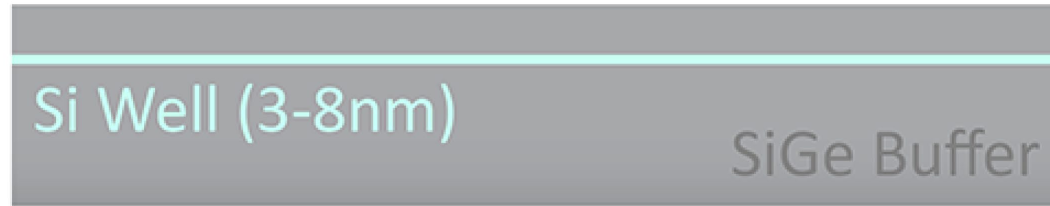
1) Uniplanar gate arrangement
   → Stronger coupling of X-gates
   → Reduced charge noise

2) Dot-shaped P-gates
   → Highly customizable gate arrangements

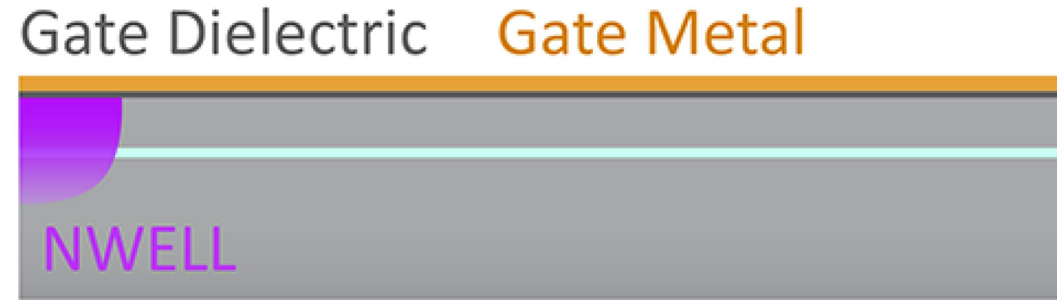
P = plunger gate
X = exchange gate
M = measure dot gate
B = bath gate

T&Z = tunnel gates
IFG = inner field gate
OFG = outer field gate

SLEDGE fabrication process flow

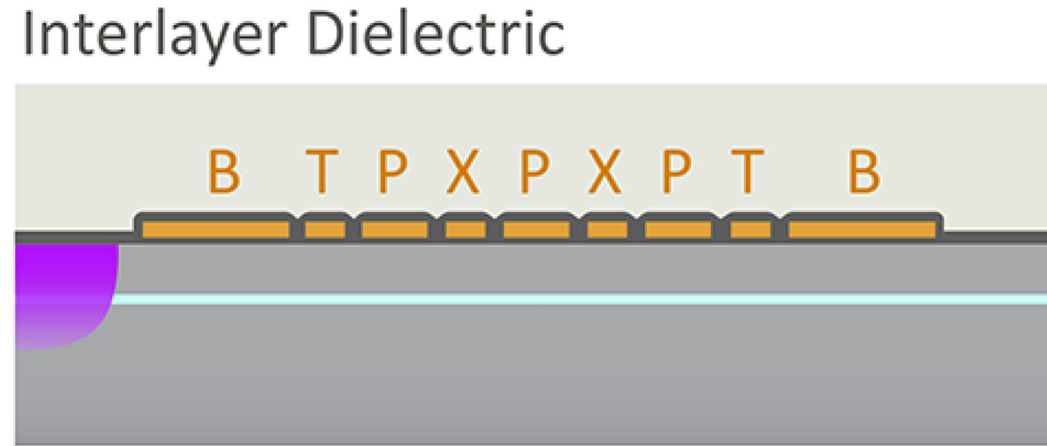


SLEDGE fabrication process flow



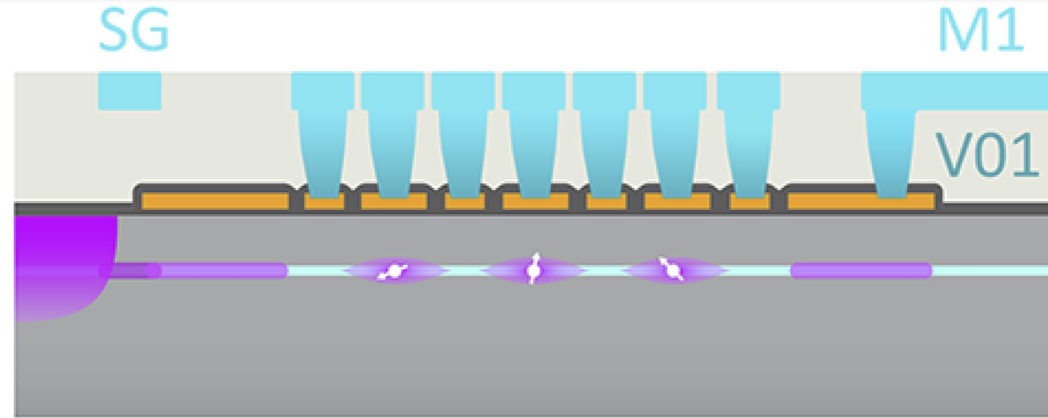
1) Formation of P-implanted Ohmics (NWELL) using optical lithography
2) Gate dielectric bilayer Al_2O_3/HfO_2
3) Gate metal TiN

SLEDGE fabrication process flow



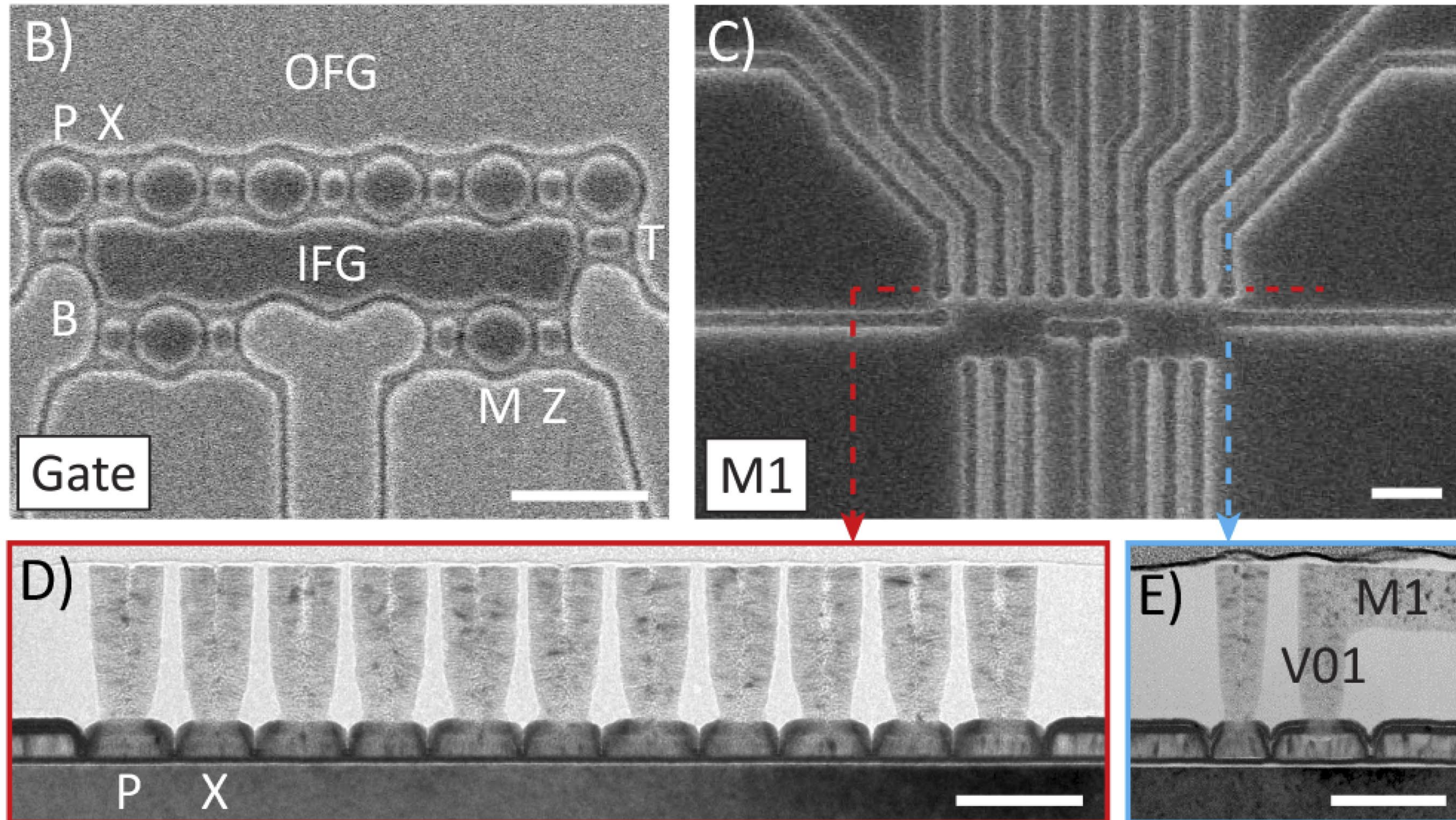
1) Two-step gate patterning:
   - coarse (optical lithography)
   - fine (positive tone e-beam lithography, F-based dry etch)
2) Etch stop (HfO_2) deposition
3) ILD (SiO_2) deposition

SLEDGE fabrication process flow



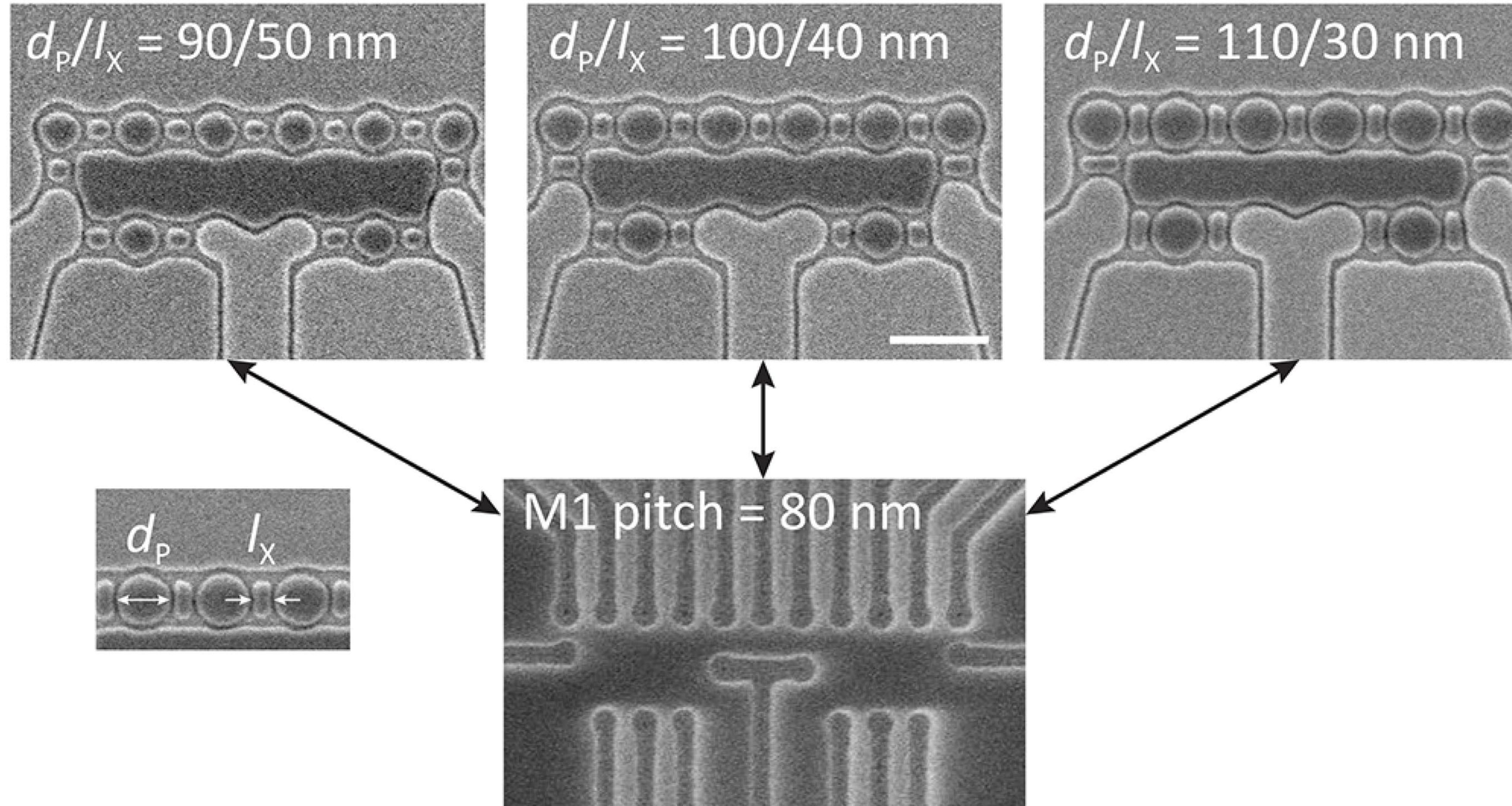
- BEOL phase: TiN dual damascene process
  1) Vias (V01) are patterned using e-beam lithography and etched into ILD
  2) M1 spans patterned by e-beam lithography, trenches etched into ILD
  3) Blanket etch to remove etch stop
  4) TiN atomic layer deposition (ALD)
  5) Chemical-mechanical polishing (CMP)

SLEDGE devices

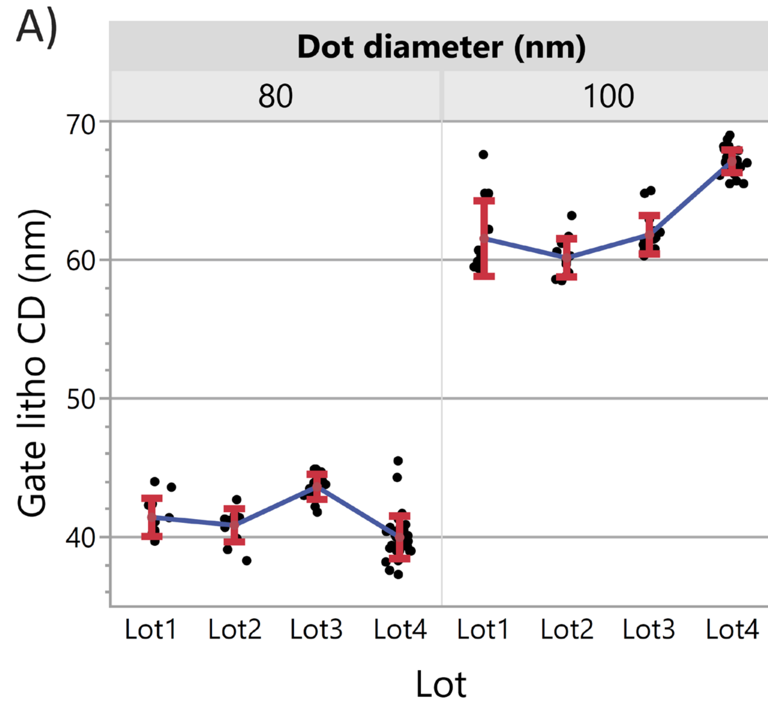


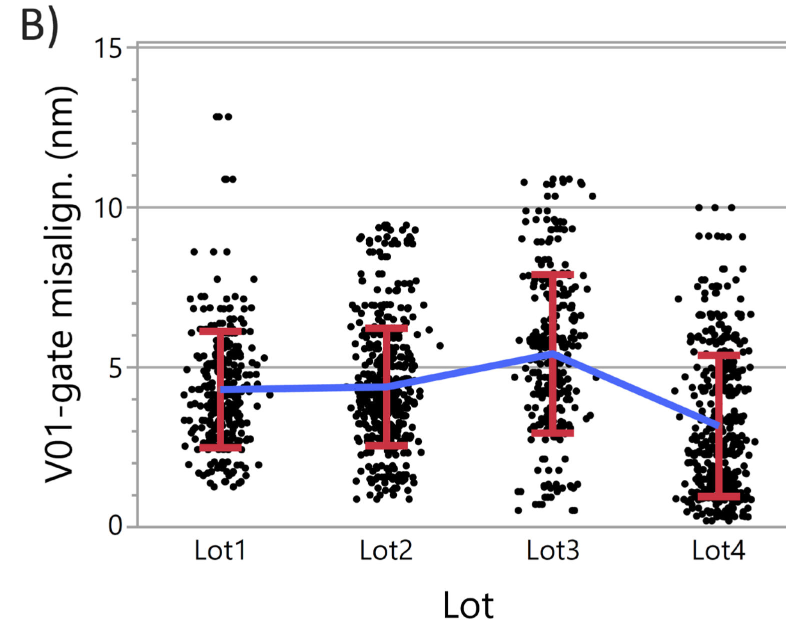
Scale bars in panels B&C (D&E) are 200 (100) nm

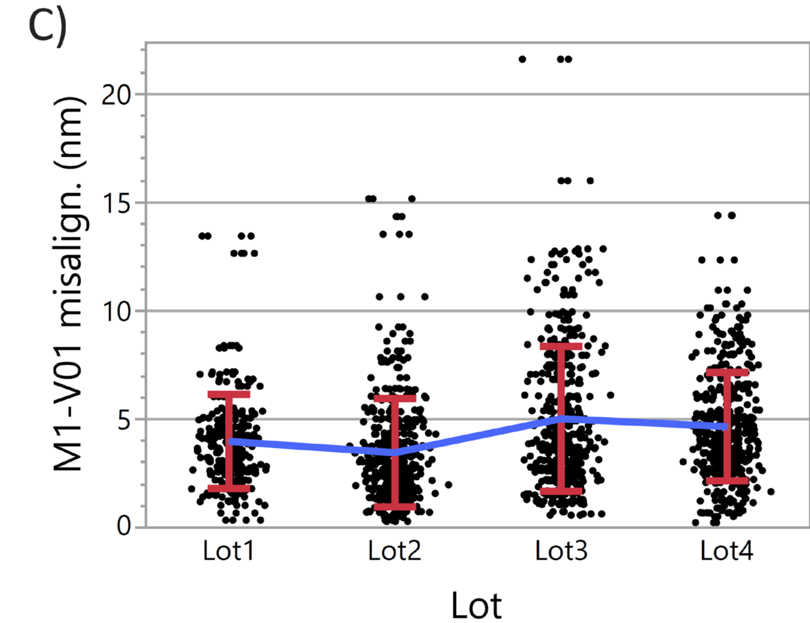
SLEDGE devices



Wafer-level reproducibility of e-beam lithography

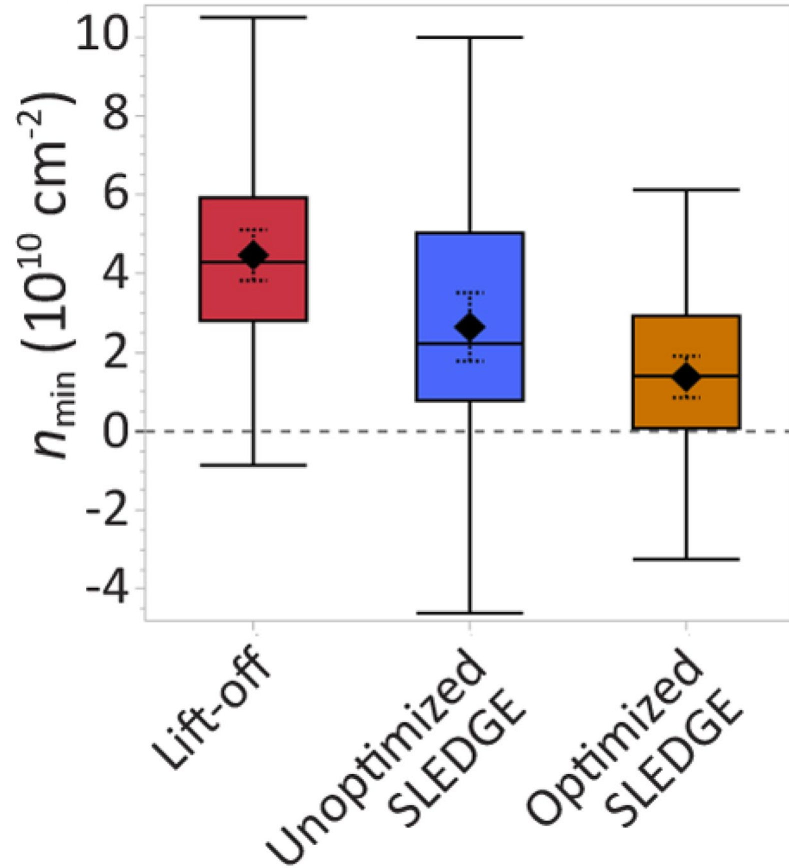






- Noncustomized, commercially available Raith EBPG5200 e-beam writer
- Misalignment magnitude $\lesssim$ 5nm (measured by an automated critical dimension SEM)
- Mean P-gate critical dimension varies less than 7%

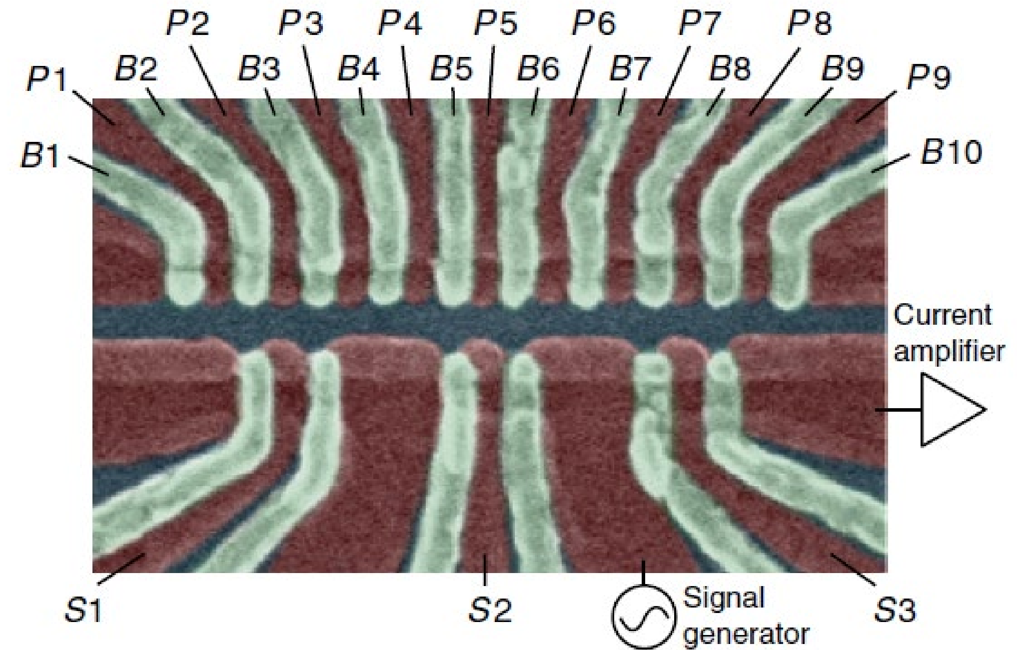
Electrostatic disorder: Hall bar measurements



n_{min} = sheet density at which the Hall mobility extrapolates to 0

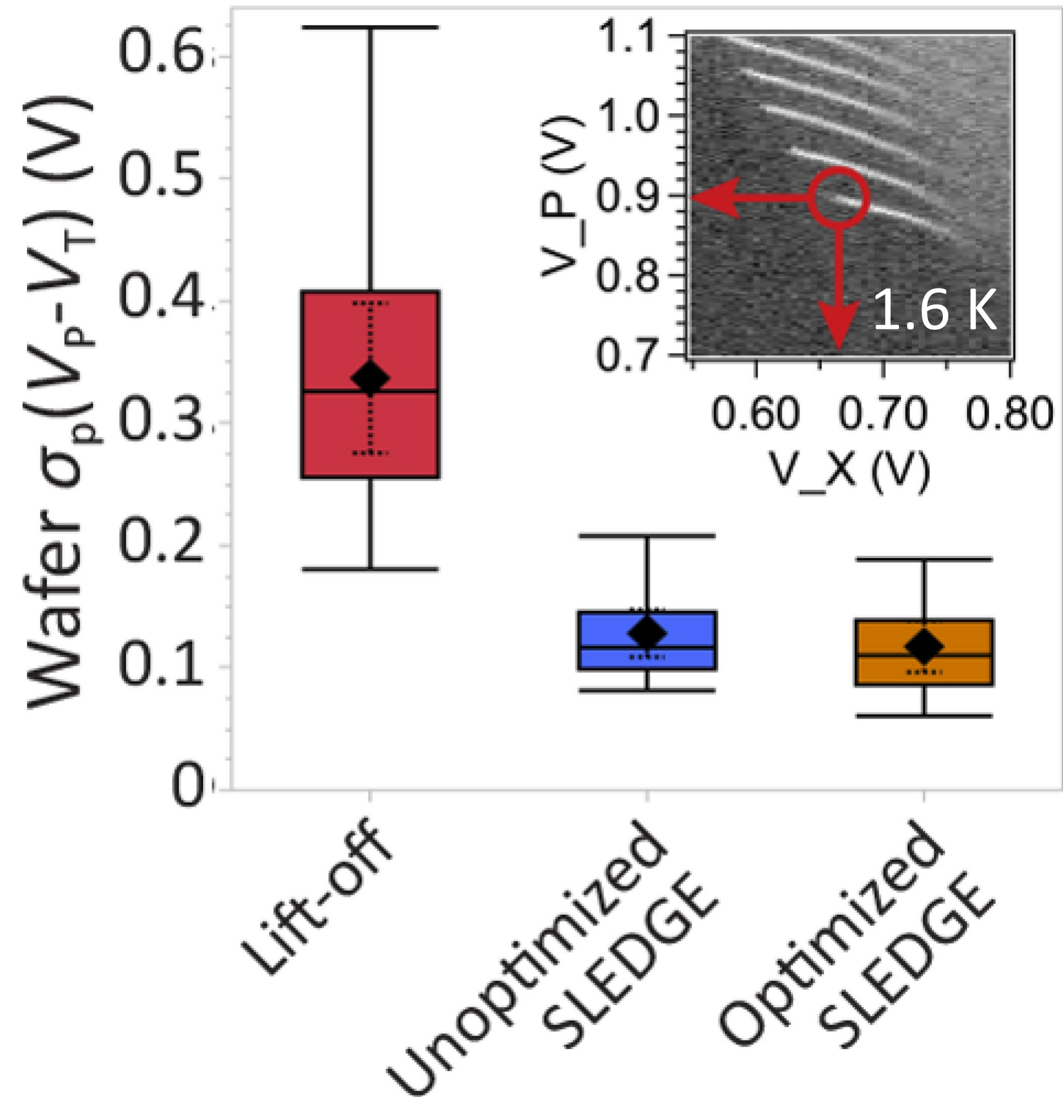
Traditional overlapping gate devices with lift-off metallization

Zajac et al., Phys. Rev. Applied 6, 054013 (2016)



Disadvantage: several dielectric layers and limited pregate clean options

Electrostatic disorder: Single-dot measurements



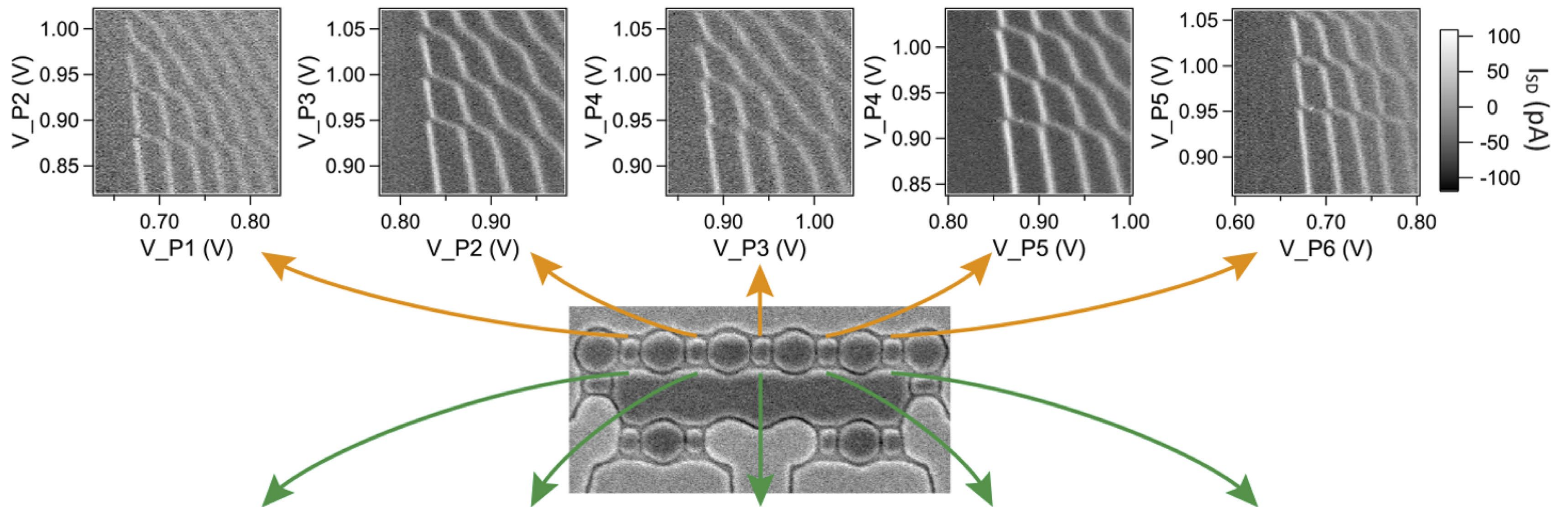
Their metric:
standard deviation of voltage difference between P- and neighboring T- or X-gates at the first electron loading line

No statistically significant difference between *unoptimized* and *optimized* (preclean) SLEDGE

→ limited by residual disorder in the gate stack

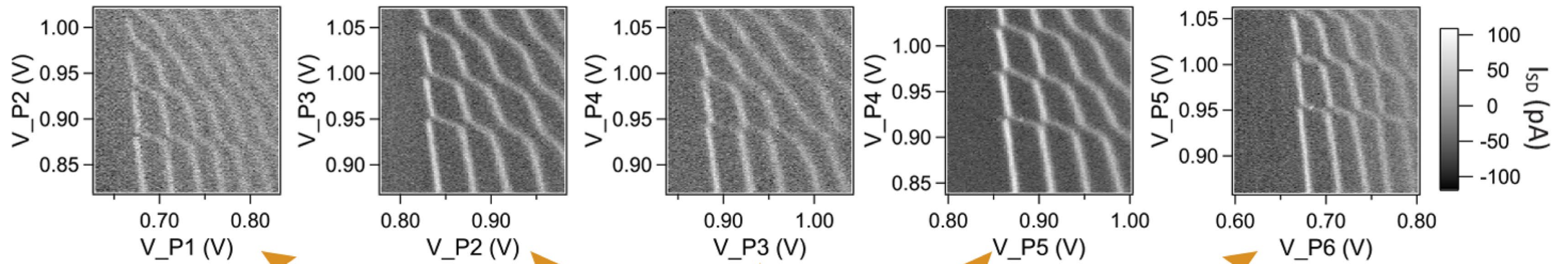
DQD charge stability diagrams

T=1.6K

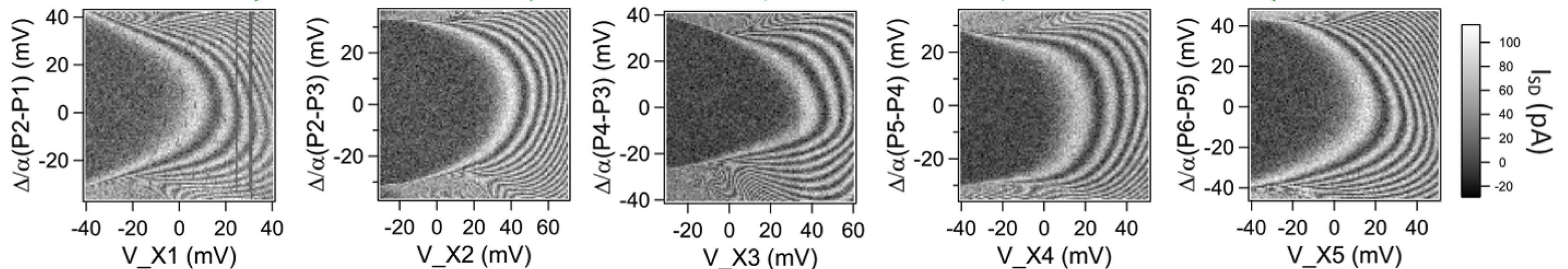


DQD charge stability diagrams and exchange oscillation fringes

T=1.6K

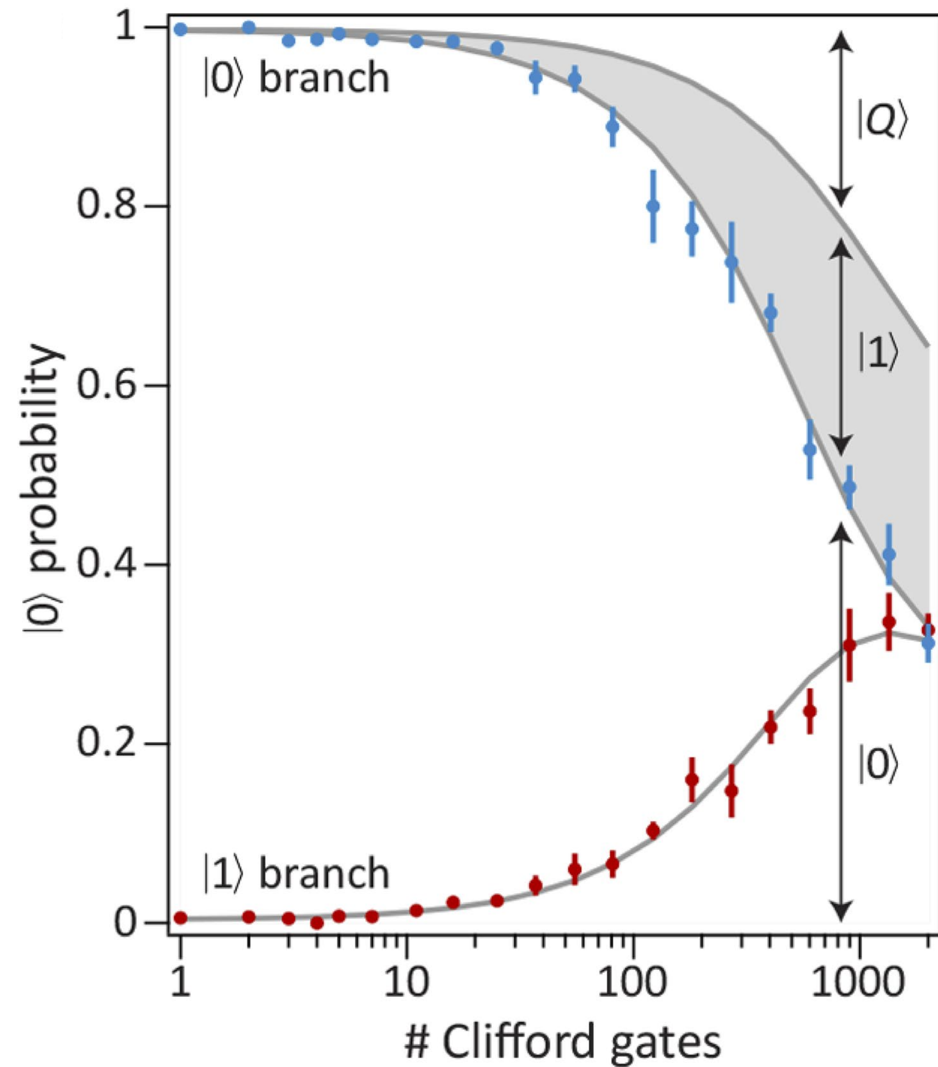


T=50mK



"fingerprint plots" see Reed *et al*., PRL 116, 110402 (2016)

Single-qubit blind randomized benchmarking



Exchange-only encoded triple-dot qubit

see also
Andrews *et al.*, Nat. Nanotechnol. 14, 747 (2019)

Per-Clifford error 0.12%
Leakage of 0.035 %