

Cryogenic hyperabrupt strontium titanate varactors for sensitive reflectometry of quantum dots

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Radio frequency reflectometry techniques enable high bandwidth readout of semiconductor quantum dots. Careful impedance matching of the resonant circuit is required to achieve high sensitivity, which however proves challenging at cryogenic temperatures. Gallium arsenide-based voltage-tunable capacitors, so-called varactor diodes, can be used for in-situ tuning of the circuit impedance but deteriorate and fail at temperatures below 10 K and in magnetic fields. Here, we investigate a varactor based on strontium titanate with hyperabrupt capacitance-voltage characteristic, that is, a capacitance tunability similar to the best gallium arsenide-based devices. The varactor design introduced here is compact, scalable and easy to wirebond with an accessible capacitance range from 45 pF to 3.2 pF. We tune a resonant inductor-capacitor circuit to perfect impedance matching and observe robust, temperature and field independent matching down to 11 mK and up to 2 T in-plane field. Finally, we perform gate-dispersive charge sensing on a germanium/silicon core/shell nanowire hole double quantum dot, paving the way towards gate-based single-shot spin readout. Our results bring small, magnetic field-resilient, highly tunable varactors to mK temperatures, expanding the toolbox of cryo-radio frequency applications.

I. INTRODUCTION

Recent years have seen rapid progress in the realization of spin qubits in semiconductors [1–4]. Hole spins in germanium (Ge) and silicon (Si) nanostructures are of particular interest thanks to the availability of all-electrical spin control [2, 5–9], short gate times [10–12], high-temperature qubit operation [13–15], intrinsically low concentration of spinful nuclei and reduced hyperfine interaction due to the p-type hole wavefunction [16] and the presence of noise sweet spots [17–19].

Fast readout of charge and spin states in semiconductor qubit devices is typically achieved using high-frequency reflectometry methods such as radio frequency (RF)-single-electron transistors [20–23], single lead sensor dots [24, 25] or gate-dispersive charge sensing [26–30]. The latter constitutes the smallest footprint charge sensing setup: The same gate that electrostatically defines a quantum dot is used to sense nearby dots. This makes gate-reflectometry the obvious choice to use with nanowire-qubits since external charge sensors are difficult to implement [31–35].

High device impedances, typically on the order of the resistance quantum $Z \geq 25.8 \text{ k}\Omega$ up to $Z \sim \text{G}\Omega$ for gate-sensors make it necessary to downconvert towards $Z_0 = 50 \Omega$ for maximizing signal and bandwidth. Down-conversion is implemented using inductor-capacitor (LC) resonators, so-called tank circuits, consisting of surface-

mount inductors and parasitic circuit or device capacitances [29]. Careful circuit design ensures optimal signal-to-noise ratios (SNRs) and high sensitivities [27, 36]. The RF characteristics of the circuits are frequently affected by cryogenic temperatures and magnetic fields required for qubit operations. Thus, in-situ tuning of the impedance matching and thereby the coupling of the RF source circuitry and the LC resonator is needed. This can be achieved using varactors [16, 24, 37–39].

Commercial varactors with high tuning range and steep capacitance-voltage (CV)-curves, classified as hyperabrupt varactors, are typically doped gallium arsenide (GaAs) diodes. Doped varactors are suitable for quantum applications only to a limited extent, requiring multiple diodes [38, 39]. This is due to freezing-out effects [39] and strong dependencies on applied magnetic fields. In particular, perfect impedance matching using GaAs varactors was so far only demonstrated down to $T \sim 200 \text{ mK}$, using two varactors [39].

To resolve these issues, quantum paraelectric materials such as strontium titanate (STO) are under consideration as alternative cryogenic varactors [40]. Below 10 K, the dielectric constant of STO ranges from $\epsilon_r = 10'000 - 24'000$ depending on the crystal orientation and was shown to be tunable with large electric fields [41–44]. Thus, STO is a prime candidate for the design of electrically tunable cryogenic RF components, such as varactors or resonators [40, 45]. The relatively small target capacitance range $C_{var} < 50 \text{ pF}$ [38] required for impedance matching makes STO varactor engineering challenging. Given the high ϵ_r , a plate capacitor formed by electrodes on opposite faces of STO crystals encounters conflicting constraints when required to reach such

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low C_{var} : i) either the capacitor plate size is too small for wirebonding or ii) the plate-to-plate distance is too large to form uniformly high fields, reducing the tunability [40]. Furthermore, contacting the electrodes on opposing faces of the crystal is inconvenient and limits scalability.

Here, we present a surface-patterned ring varactor design on STO which achieves hyperabrupt CV characteristics and a tuning range exceeding that of typical GaAs varactors [24, 38, 39] while operating down to mK temperatures and independent of magnetic fields. We fabricate varactors of various dimensions and characterize them first at 4 K, optimizing for tunability and capacitance range.

Next, we integrate such a varactor in a tank circuit for gate-dispersive readout. The selected design has a $300\ \mu\text{m}$ footprint, smaller than STO plate-capacitor layouts and packaged commercial varactor diodes. Critical coupling is reached over a broad range of temperatures from $T \approx 4\ \text{K}$ to $11\ \text{mK}$ to and in magnetic fields up to $2\ \text{T}$ without retuning of the varactor. We use the matched circuit to dispersively measure charge transitions in a hole double quantum dot (DQD) formed in a Ge/Si core/shell nanowire (NW) [46–49]. Similar NWs were used to demonstrate all-electrical, ultrafast spin qubit operation with a high degree of tunability [6–8, 10]. To directly probe the significance of impedance matching for gate-dispersive charge sensing, we measure signal-to-noise ratios (SNRs) for variable matching conditions and at different charge transitions. Our implementation of gate-dispersive charge sensing paves the way for high-fidelity gate-dispersive single-shot spin readout with gated quantum dots (QDs). The realization of a highly tunable capacitor at cryogenic temperatures enables more sophisticated circuit architectures in various applications beyond charge sensing in semiconductors.

II. VARACTOR CHARACTERIZATION AT 4 K

A. Geometry

The varactor ring design is presented in Fig. 1 a). It features two electrodes, a central circle with diameter D and a concentric ring, $50\ \mu\text{m}$ wide and separated from the circle by a distance w . A gap $g = 20\ \mu\text{m}$ wide in the outer ring facilitates lift-off. The electrodes were patterned on the polished side of a commercially available (001) STO chiplet with thickness $t = 0.5\ \text{mm}$ (Appendix A 1). This geometry provides several key features for optimal varactor performance: electric fields in the crystal are localized and large close to the electrodes. This allows for high tunability of ϵ_r while keeping the peak capacitance C_{max} in the desired range. The small varactor footprint of $\sim 300\ \mu\text{m}$ and single-sided metallization allows tight integration with other circuit components and provides scalability. In particular, we are able to fit 9 independent ring varactors on a chiplet the size of commercial surface-mount GaAs varactors used in comparable experiments

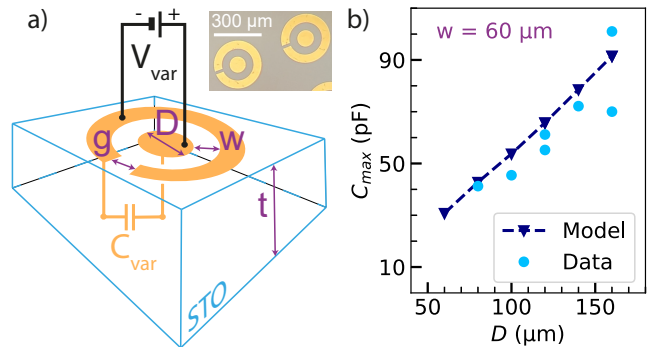


FIG. 1. **Geometry of STO ring varactors** a) Schematic diagram of the STO varactor design. Two gold electrodes, a circle with diameter D and a concentric ring with a spacing to the circle w and gap $g = 20\ \mu\text{m}$ form the capacitor. Application of a DC voltage V_{var} induces an electric field within the STO crystal which is highly localized due to the compact geometry. Inset: Optical micrograph of finished varactors. b) Zero-field capacitance C_{max} as a function of D for $w = 60\ \mu\text{m}$, simulated in COMSOL (triangles) and measured (circles). Spread of measured data partly due to unintentional negative V_{var} hysteresis effects (see text).

(MACOM MA46-series) [24, 38, 39].

All measurements presented in this section were performed at 4 K using standard lock-in techniques at 1 kHz. No frequency dependence of tunability and ϵ_r from 1 kHz to 50 MHz was reported previously, predicting constant ϵ_r up to 100 GHz [43]. We thus expect our low-frequency results to apply at typical reflectometry frequencies as well. We estimate the zero-field capacitance C_{max} of our design using *COMSOL* to find optimal device dimensions. For simplicity, we assume an isotropic dielectric constant $\epsilon_r = 24'000$, approximately the experimental value for field lines parallel to the (001) direction at 4 K [43]. In our simulation, we primarily focus on D and w , finding that neither g nor the width of the outer ring have a strong influence on C_{max} . We vary D from $60\ \mu\text{m}$ to $160\ \mu\text{m}$ and w from $10\ \mu\text{m}$ to $80\ \mu\text{m}$ and fabricate an array of 36 different combinations, excluding $w > 60\ \mu\text{m}$ due to decreased tunability. Not all combinations were measured because too small w and D frequently resulted in shorts between the two electrodes from wirebonding (see Appendix C 1 for details).

In Fig. 1 b), we compare the zero-field capacitance C_{max} estimated from finite-element simulations and measurements for $w = 60\ \mu\text{m}$ and variable D . We find good agreement, noting that some small capacitance over-estimations by the model could be explained by the anisotropy of ϵ_r , which was neglected in the simulation. Furthermore, the hysteretic effect described in II B and Fig. 2 c) may also explain some of the measured C_{max} lying below the model, as some of these values were taken from voltage sweeps starting at a varactor voltage $V_{var} = -2\ \text{V}$.

B. Voltage-Tunability

The CV-characteristic of a diode varactor near its peak tunability regime can be expressed as

$$C_{var}(V_{var}) = \frac{K}{(V_{var} + \Phi_{diode})^\gamma} \quad (1)$$

where K is the capacitance constant, V_{var} is the applied varactor voltage, Φ_{diode} is the built-in potential of the varactor and γ is the power law exponent [50]. Abrupt varactors have $\gamma \leq 0.5$ and if $\gamma > 0.5$ the varactor is considered hyper-abrupt. For GaAs varactors, $\Phi_{GaAs} = 1.3$ V holds [51].

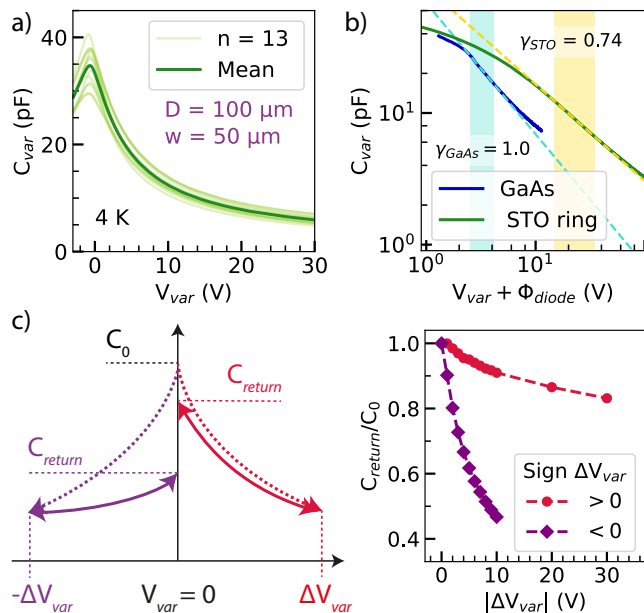


FIG. 2. **CV-Characteristic** a) Varactor capacitance C_{var} as a function of applied DC voltage measured on 13 nominally identical devices (light green) and mean value (dark green). b) Comparison of the capacitance-tunability of a commercial GaAs varactor with one exemplary STO ring at 4 K. The yellow (turquoise) dashed lines are fits to the steepest regime of the STO (GaAs) CV-traces, indicated by the shaded areas. c) Schematic image (left panel) and quantitative analysis (right panel) of the varactor tunability hysteresis. Applying negative V_{var} (purple diamonds) causes a significant degradation of the capacitance tunability which is less severe for positive V_{var} (red circles).

From now on, we focus on devices with $D = 100 \mu\text{m}$ and $w = 50 \mu\text{m}$ as these varactors covered the desired capacitance range and could be easily bonded. CV-characteristics of 13 nominally identical devices are shown in Fig. 2 a) & b), revealing approximately 10% variability from the mean. The peak capacitance C_{max} is found at moderately negative voltages $V_0 \approx -0.7$ V. We thus use $\Phi_{STO} = 0.7$ V in the fit of the CV data to equation (1) to extract γ . For all 13 devices, we find hyperabrupt behavior over a large voltage range with mean $\bar{\gamma}_{STO} = 0.72 \pm 0.05$ as shown in Appendix C.2.

To minimize the hysteretic effect discussed in the following, we measure a single varactor from $V_{var} = 0$ V to $V_{var} = 100$ V as shown in 2 b). The accessible capacitance range of the STO varactor is $C_{var} = 45.0$ pF to 3.2 pF, exceeding the range of a commercial GaAs device used in comparable experiments (*MACOM* MA46H204-1056) [24, 38, 39] and of previous STO plate-capacitor implementations [40].

Interestingly, varactors with identical geometry but fabricated on (100) and (111) STO showed no significantly different CV-response as compared to the (001) devices. While (100) is equivalent to the (001) direction, the zero-field dielectric constant of (111) STO is $\epsilon_r = 12000$ [43], half the value of (001) STO. The approximately circular symmetry of the surface-electrode evenly integrates over all field directions in the crystal plane, effectively averaging away the anisotropy in ϵ_r .

Sweeping from $V_{var} = 0$ V to a finite voltage ΔV_{var} , we observe a reduction in C_{var} from C_0 to C_{return} (Fig. 2 c)). The reduction is strongly dependent on the sign of ΔV_{var} as defined in Fig. 1 a). Negative ΔV_{var} cause significantly bigger losses than positive ΔV_{var} . This hysteretic effect is quantified in the right panel of Fig. 2 c), where C_{return}/C_0 is measured by sweeping to increasingly large $|\Delta V_{var}|$ and back to zero. In subsequent cycles between $V_{var} = 0$ V and ΔV_{var} , the CV-characteristic remains stable. The lost tunability is fully recovered upon thermal cycling to 295 K. A similar degradation of tunability observed in a low-impedance resonator on STO has been attributed to reordering of *O*-vacancies near the surface electrode [45]. The residual degradation of tunability present even when only applying positive voltages can easily be circumvented by choosing appropriate varactor dimensions and limiting the range of voltages applied.

III. GATE-DISPERSIVE CHARGE SENSING WITH GE/SI CORE/SHELL NANOWIRE DOUBLE QUANTUM DOTS

A. Impedance Matching

In a next step, we implement gate-dispersive charge sensing with a Ge/Si core/shell NW hole DQD, using a STO varactor to optimize impedance matching. See Appendix A 2 for NW device fabrication details. Quantum dots hosted in these NWs have been measured in direct current (DC) measurements [47, 48, 52–55], using additional quantum dots as charge sensors [31, 32] and with an on-chip superconducting resonator [35, 56]. A strong, electrically tunable direct Rashba spin-orbit interaction (SOI) is present in Ge/Si core/shell NWs [6–8, 48], enabling all-electrical spin control. Recent spin qubit experiments in this system have shown Rabi frequencies of several hundreds of MHz [10].

The reflectometry setup used to integrate an STO ring varactor with the NW device shown in Fig. 3 a) is de-

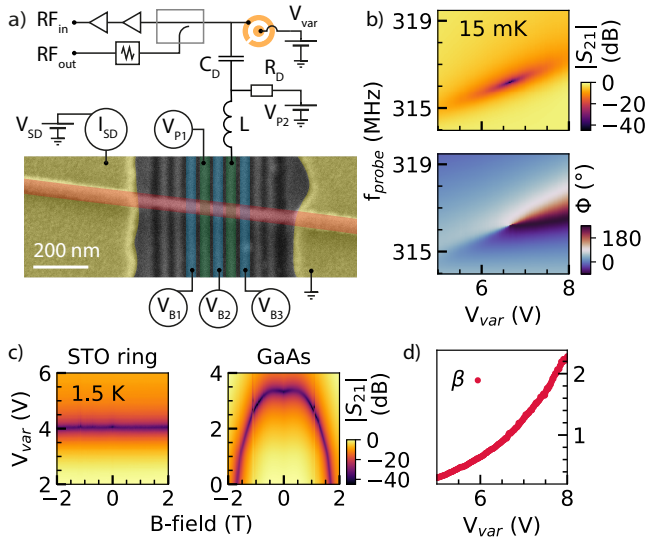


FIG. 3. Reflectometry setup and Impedance Matching
a) Gate-reflectometry circuit with STO matching-varactor. The false-colored SEM image shows a NW device with nine gates, five of which were used to form a DQD with two plungers (green) and three barrier gates (blue). The NW (red) is contacted on either side, enabling DC-current measurements through the wire. b) Impedance matching at probe temperature $T_{probe} \approx 15$ mK. At perfect matching, the reflected amplitude is minimal and the phase response indicates a sudden shift from undercoupled ($V_{var} < 6.625$ V) to overcoupled ($V_{var} > 6.625$ V). c) Magnetic field-dependent impedance matching at $T \approx 1.5$ K without NW device. The tank with a STO ring varactor is unaffected by magnetic fields up to 2 T. Using a GaAs varactor, the matching voltage shifts strongly, complicating qubit measurements. d) Coupling coefficient β as a function of V_{var} .

scribed in more detail in Appendix B. The tank resonance frequency at $f_{res} = 316.20 \pm 0.05$ MHz allows us to extract the parasitic capacitance $C_p = 1.15 \pm 0.03$ pF of the circuit. Tuning the tank as shown in Fig. 3 b), we reach impedance matching at probe temperature $T_{probe} \approx 15$ mK in a *Bluefors* dilution refrigerator. We find the STO varactor to be highly temperature-resilient (Appendix C 3). The resonator coupling coefficient β is depicted in Fig. 3 d) [39]. The transition from the under- ($\beta < 1$) to overcoupled regime ($\beta > 1$) is marked by a narrow minimum in the reflected amplitude $|S_{21}|$ where perfect matching ($\beta = 1$) is reached.

The impact of an in-plane magnetic field on the matching with STO ring varactors and commercial GaAs varactors is compared in Fig. 3 d). Both scans were recorded at 1.5 K because the GaAs varactor froze out at lower temperatures. No NW device was present for both scans. Fixing f_{probe} near resonance at zero field, B is subsequently swept against V_{var} . The GaAs varactor shows a strong dependence on B even for $B \leq 1$ T, the typical spin qubit operation range [2, 3, 5, 8, 13]. The STO remains independent of B-field down to mK temperatures (Appendix C 4).

B. Charge Sensing

Finally, we investigate charge transitions in a Ge/Si core/shell NW DQD using the impedance-matched tank circuit. Five bottom gates were used to define a DQD (Fig. 3 a)). Bias triangles, the hallmark signature of a DQD, are shown in Fig. 4 a). Due to Coulomb-blockade, source-drain current I_{SD} can only flow through the DQD if at least one quantized energy level of each dot lies within the bias window. Estimating the plunger gate lever arms from the DC bias triangle yields $\alpha_{P1} \approx 0.3$ and $\alpha_{P2} \approx 0.24$ for the gates $P1$ and $P2$, respectively, in line with previous results on bottom-gated devices [47].

Gate-reflectometry allows for the measurement of tunneling between the dots (interdot transition) as well as between the dot under the sensor gate and a neighbouring reservoir (lead transition). Simultaneously measuring I_{SD} and changes of the reflected RF amplitude $\Delta|S_{21}|$ and phase $\Delta\Phi$ demonstrates the correspondence of the two signals. In the reflectometry signal, the two reservoir transitions (white in $\Delta\Phi$) and the interdot transition (dark purple in $\Delta\Phi$) are clearly visible, appearing similarly in both $\Delta|S_{21}|$ and $\Delta\Phi$ signals. Note that the phase jumps by more than $|\Delta\Phi| = 10^\circ$ at the transitions due to the close to perfect matching. In addition, the excited state also appears faintly between the reservoir lines, plus a weak copy of both ground and excited state transitions below the the lower reservoir transition. The visibility of such features depends intricately on the balance of the tunnel barriers and the resulting tunnel rates in comparison to the resonator frequency. We note the remarkable stability of the quantum dots which can be formed in these NWs, manifesting in very sharp and highly repeatable transitions (see also Appendix D), only sporadically interrupted by a random charge switcher. A large-scale charge stability map is presented in Appendix D alongside investigations into the tunability of interdot tunneling using the barrier gate $B2$.

For the following analysis of lineshapes and SNRs, we measure at zero source-drain bias to reduce random charge switchers and maximize dispersive signal. We select a lead transition which shows up primarily in the reflected phase and a bright interdot transition near the triangle depicted in Fig. 4 a). The lead transition lineshape can either be dominated by the reservoir hole temperature T_H , exhibiting a \cosh^{-2} -dependence on the gate voltage, or by tunnel-broadening which results in a Lorentzian lineshape with a tunnel rate γ_L [57]. Fitting the particular transition depicted in Appendix E 1, we find slightly better agreement of the tail region with a \cosh^{-2} -relation, hinting towards the temperature broadened regime, i.e. that $k_B T_H > \hbar\gamma_L$ with k_B Boltzmann's constant and \hbar the reduced Planck's constant. We can thus extract $T_H \approx 520 \pm 20$ mK. This temperature is far above the refrigerator temperature, presumably due to microwave irradiation from the cryogenic amplifier. The interdot tunnel coupling $t_c \approx 22 \pm 5$ μ eV can be extracted fitting the interdot transition shown in Appendix E 2. See

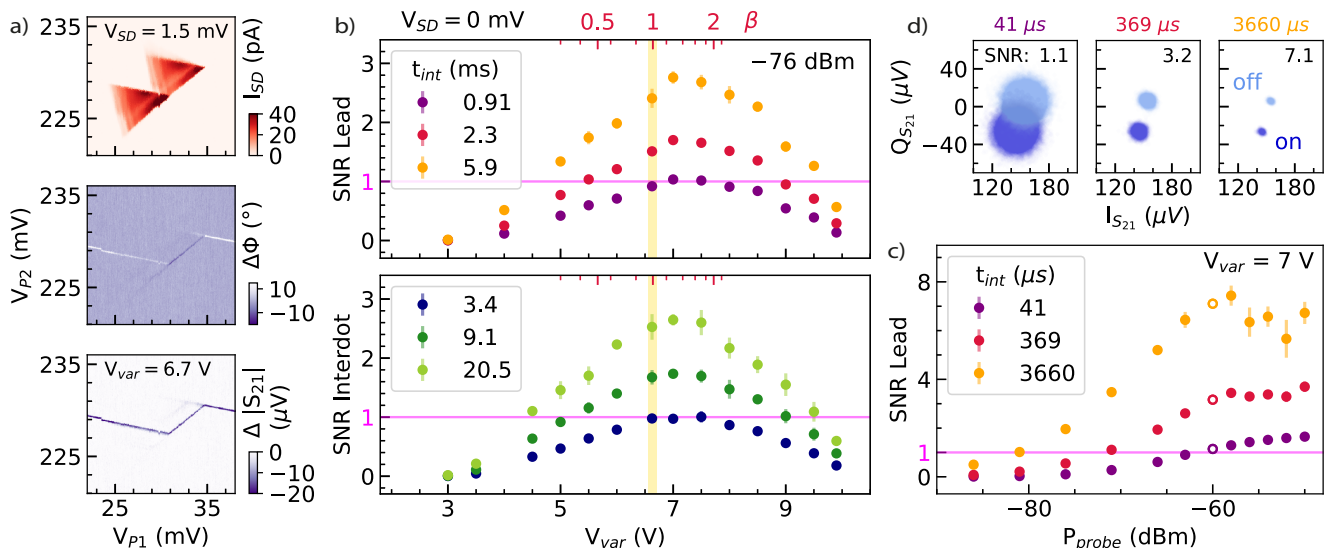


FIG. 4. **Sensing a Ge/Si NW DQD** a) Charge stability map of a DQD formed in the Ge/Si core/shell NW, showing a characteristic bias triangle in the DC-current measurement (top). The simultaneously acquired reflectometry data (middle & bottom) feature an interdot line coinciding with the triangle baseline and lead transitions of the right dot with its reservoir. b) Time-domain SNR measurements of similar transitions as in a) as a function of V_{var} and integration time t_{int} . Both transition SNRs behave similarly: The highest SNR regime is shifted to higher V_{var} from the perfect matching (yellow shaded region). Investigating the interdot line, longer integration times are required to cross the SNR = 1 threshold (pink). Five independent SNR measurements were taken for each V_{var} . Error bars represent one standard deviation. c) The SNR can be increased by applying higher powers up to approximately $P_{probe} = -58$ dBm where the signal saturates. d) Demodulated data measured on (dark blue) and off (light blue) the lead transition at $P_{probe} = -60$ dBm, corresponding to the empty circles in c).

Appendix E for estimates of the quantum capacitances associated with these transitions [57]. Power broadening sets in above $P_{probe} \approx -60$ dBm for both transitions mentioned, resulting in a reduced signal amplitude and larger width.

We investigate the impact of impedance matching through time-domain SNR measurements [28] at the two transitions mentioned above. Note that a random charge switcher occurred before we started the SNR measurements, resulting in a lower signal for the interdot transition than in the lineshape-investigation. We record time-traces of the demodulated reflectometry signal on and off a given charge transition for 2 s with a lock-in time constant $TC = 4 \mu\text{s}$. The in-phase ($I_{S_{21}}$) and quadrature ($Q_{S_{21}}$) components are then binned for a variable integration time t_{int} . Fig. 4 d) depicts the two signals on the IQ -plane for different t_{int} . Comparing the distance of the two signals with the spread of the points estimates the SNR [28].

Fig. 4 b) shows the SNRs measured as a function of V_{var} . The need for longer integration at the interdot transition may be due to different tunnel rates. Both transitions exhibit the same qualitative dependence of SNR on V_{var} . The best SNR is in the slightly over-coupled regime at $V_{var} \approx 7$ V where $\beta = 1.28$. In the case of dispersive sensing of a reactive load, the reduction of C_{var} by increasing V_{var} may lead to a higher tank quality factor thus shifting the optimal sensing configuration away from perfect impedance matching [39]. The

observed shift of the tank resonance towards higher frequencies in 3 b) supports this hypothesis. Evidently, the ability to tune impedance matching is of major importance for SNR optimization. Detuning the varactor by $\Delta V_{var} = 2$ V from the best operation point, causing a capacitance change of $\Delta C_{var} = \pm 4$ pF, the SNR drops by up to a factor of ~ 2 .

The power-dependence of the SNR at the lead transition for $V_{var} = 7$ V is shown in 4 c). We find that $P_{probe} > -60$ dBm causes significant instability of the system, as seen from the higher errors and plateauing of SNR, consistent with the onset of power broadening of the charge transitions (Appendix E). At $P_{probe} = -60$ dBm, $t_{int} = 41 \mu\text{s}$ suffices to achieve SNR = 1.1 (see Appendix D 3 for charge stability maps at low TC).

IV. CONCLUSION AND OUTLOOK

In conclusion, we have fabricated and characterized hyperabrupt STO varactors with more than one order of magnitude tuning range. These varactors are not affected by moderate magnetic fields and can operate down to low mK temperatures. The small size allows tight integration with other PCB components and scaling in applications with multiple tunable capacitors such as multiplexed readout. We demonstrate the high-frequency functionality of these varactors for gate-dispersive sensing of a Ge/Si core/shell NW hole DQD.

These results open the possibility for gate-dispersive single shot readout of spins in Ge/Si core/shell NWs and spin-relaxation measurements. Increasing the sensor gate lever arm as well as the resonator quality factor are important steps to improve the signal further. Expanding the varactor design, more elaborate matching networks including two tunable capacitors in one device may allow for greater flexibility and voltage-tunability of the tank resonance frequency. In particular, lowering C_{max} while keeping γ similar should enable impedance matching with high-Q superconducting inductors.

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AUTHOR CONTRIBUTIONS

R.S.E, T.P. and D.M.Z conceived of the project and planned the experiments. R.S.E. and D.T. fabricated and measured the STO varactors with inputs from T.P.. S.S. fabricated, tuned and operated the NW device. M.J.C. and P.C.K. helped with the NW device fabrication. R.S.E and S.S. integrated the varactor with the NW device and implemented the charge sensing experiments with inputs from T. P.. R.S.E, S.S., D.T. and T.P. analyzed the data with inputs from M.J.C., S.G., A.V.K. and D.M.Z.. A.L. and grew the NWs under the supervision of E.P.A.M.B.. R.S.E. wrote the manuscript with inputs from all authors. D.M.Z. supervised the project.

COMPETING INTERESTS

The authors declare no competing interests.

Appendix A: Device Fabrication

1. Varactor fabrication

The STO ring varactors were optically defined using a Heidelberg μ PG laser-writer to pattern the structures on a commercially available SrTiO₃ (001) wafer (refractive index $n = 2.39$) [40]. The STO chiplets used were

0.5 mm thick, single-side polished, with a TiO₂ termination on the back side, purchased from *SurfaceNet*. A bilayer of photoresist, consisting of LOR 3A and S1805, was used. The laser-writer was operated in pneumatic focusing mode due to the optical transparency at the wavelength of 405 nm. The structures were metallized with 5 nm/65 nm of Ti/Au. On one 10×10 mm² chip, approximately 200 devices were co-fabricated and cleaved into smaller segments with 5 – 15 varactors for wirebonding and PCB integration.

2. Nanowire device fabrication

The QD device featured a set of 9 bottom gates with a width of 20 nm and a pitch of 50 nm. The gates were fabricated by electron beam lithography (EBL) on an intrinsic Si (100) chip with 290 nm of thermal SiO₂. Upon cold development [58] the gates were metallized with 1 nm/9 nm of Ti/Pd, respectively. In order to electrically insulate the gates from the NW, the gates were covered by a ~ 20 nm thick layer of HfO₂ grown by atomic layer deposition. A single Ge/Si core/shell NW with core radius of ~ 10 nm and a shell thickness of ~ 2.5 nm [46] was deterministically placed approximately perpendicular to the 9 bottom gates. However, the exact in-plane angle is unknown. Finally, ohmic contacts were patterned by EBL and metallized with 0.3 nm/50 nm of Ti/Pd after a 10 s dip in buffered hydrofluoric acid to remove the native SiO₂. The scanning electron micrograph presented in Fig. 3 shows a co-fabricated device.

Appendix B: Reflectometry setup

A STO varactor with $D = 100 \mu\text{m}$ and $w = 50 \mu\text{m}$ was integrated into a standard reflectometry setup shown in Fig. 3 a) on a printed circuit board (PCB). Attenuated coaxial cables were used to inject an RF tone at frequency f_{probe} via a directional coupler (*Mini-Circuits* ZX30-17-5-S+) into a bias tee on the PCB ($C_D = 87$ pF, $R_D = 5$ k Ω). The varactor was operated as a tunable shunt-capacitor. A surface mount ceramic core inductor $C_D = 220 \pm 6$ nH, in series with the parasitic capacitance of a bottom gate of the NW device formed the tank circuit. From the resonance frequency $f_{res} = 316.20 \pm 0.05$ MHz we find a parasitic capacitance $C_p = 1.15 \pm 0.03$ pF. Filtered DC lines were used to provide gate-, source-drain bias- and varactor voltages. The reflected signal was amplified at the 4 K stage (*Low Noise Factory* LNC0.2-3A) and at room temperature (*B&Z* BZY-00100700). A *Zurich Instruments* UHFLLI Lockin amplifier was used for signal generation and demodulation at room temperature. DC voltages were provided by a *Basel Precision Instruments* SP927 digital to analog converter and I_{SD} was amplified by a *Basel Precision Instruments* SP983c current to voltage converter

and recorded using an *Agilent* 34410A digital multimeter.

Appendix C: Varactor properties

1. Geometry

The results of COMSOL simulations of the C_{var} -dependence on D and w are shown in Table I.

TABLE I. Simulated C_{var} at $V_{var} = 0$ V in pF

$D \setminus w$ (μm)	10	20	30	40	50	60	70	80
60	43	36	34	32	31	31	30	30
80	62	52	48	45	43	42	42	40
100	79	68	61	58	56	54	53	52
120	97	86	75	72	68	66	65	63
140	117	102	91	85	81	79	77	75
160	135	120	106	99	94	92	89	86

Corresponding measurements at $T = 4$ K are shown in Table II. Note that only devices with $w \leq 60$ μm were fabricated and for small w and D , measurements were often impossible because wirebonding created shorts between the two electrodes. Typical room-temperature capacitances were ≤ 1 pF to 1.5 pF. In a few cases, the room-temperature capacitance was exceeding 10 pF, likely originating from the DC wiring. These offsets were subtracted from the measured 4 K data presented here. Note that two such cases were excluded from the variability analysis in the main paper.

TABLE II. Measured C_{var} at $V_{var} = 0$ V in pF

$D \setminus w$ (μm)	10	20	30	40	50	60
80	-	-	-	-	36	41
100	-	79,43	52	-	43	46
120	45	-	-	-	-	55,61
140	-	-	69	-	78	74
160	-	88,83	80	46	74,27	73,97

To assess the tunability range, we present the measured values of C_{var} at $V_{var} = 30$ V in Table III.

TABLE III. Measured C_{var} at $V_{var} = 30$ V in pF

$D \setminus w$ (μm)	10	20	30	40	50	60
80	-	-	-	-	13	12
100	-	24,18	19	-	14	15
120	20	-	-	-	-	21,21
140	-	-	25	-	23	25
160	-	26,72	28	15	18,30	29,26

These limitations with regards to wirebonding should be easily overcome by adapting the electrode design to include remote, designated bondpads. This would make

the smaller capacitance values listed in Table III accessible without severe reduction of tunability. Furthermore $C_{var} \sim 1$ pF at $V_{var} = 0$ V may be reached if the dimensions of the ring are further reduced which would allow for different tank topologies and [36] and tuning of the impedance matching with superconducting inductors.

2. Variability of hyperabrupticity

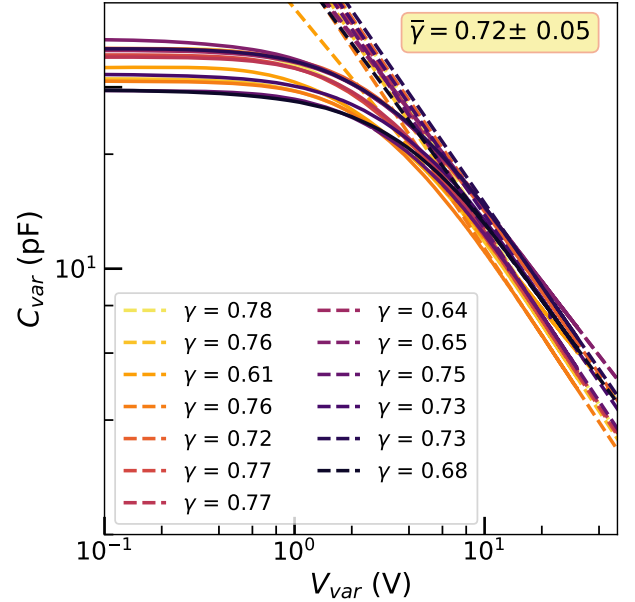


FIG. 5. Fits of CV-traces for all 13 devices from main Fig. 2 a)

All 13 devices depicted in main text Fig. 2 a) show hyperabrupt CV-characteristics, as demonstrated in the fits shown in Fig. 5. We find the mean power-law exponent to be $\bar{\gamma} = 0.72 \pm 0.05$.

3. Temperature-dependence of matching

Fig. 6 shows the tank resonance recorded in the *Bluefors* setup for a fixed V_{var} using an STO varactor and, for comparison, using a GaAs varactor diode (*MACOM* MA46H204-1056)[36, 38]. The STO varactor has almost no temperature-dependence below 4.3 K down to 11 mK. The GaAs varactor, in contrast shows a strong dependence on the temperature which sets in around 53 K, making perfect matching impossible in the mK regime.

4. Zero-field anomaly

In the *Bluefors* LD setup, we observe a shift of the optimal matching condition within a range of $B \approx \pm 50$ mT

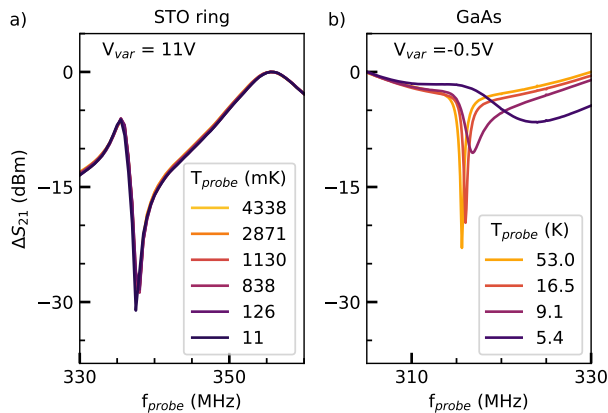


FIG. 6. **Temperature-dependence of the tank resonance** Two subsequent cooldowns of the sample PCB without NW device in the *Bluefors* setup with a) an STO ring varactor and b) a commercial GaAs varactor used to tune impedance matching.

from $B = 0$ T as shown in Fig. 7.

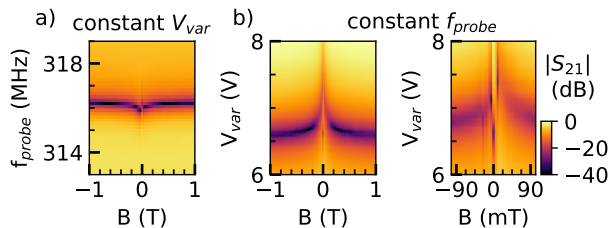


FIG. 7. **Zero-field anomaly** a) Shift of the tank resonance near zero field while V_{var} is kept constant. b) The effect is visible much more prominent in a scan at constant f_{probe} , sweeping V_{var} . The right panel is a zoom-in on the low-field regime. Note the apparent discontinuities at $B < 10$ mT.

The origin of this shift remains elusive. Scans where V_{var} is ramped rather than f_{probe} show a stronger effect. The measurements presented in Fig. 3 show only a minor feature at $B = 0$ T. There are three apparent reasons for this discrepancy:

First, it is possible that the STO varactor tunability/dielectric constant is affected in a different manner at $T \approx 15$ mK as compared to $T \approx 1.5$ K. Since no such dependence was mentioned in previous work [40], this appears to be a less likely explanation.

Second, the cryogenic amplifiers used in the two setups were different, namely a *Cosmic Microwave* CLTF2 was used in the measurements at 1.5 K (similar as CLTF1 used in [40]), but the setup at 15 mK featured a *Low Noise Factory* LNC0.2-3A amplifier.

Third, the wirebonds used to bond the varactor are aluminium, whose normal-superconducting transition might show up around these fields. Further experiments are needed to finally exclude or confirm either hypothesis.

Appendix D: Charge sensing

1. Charge-stability maps

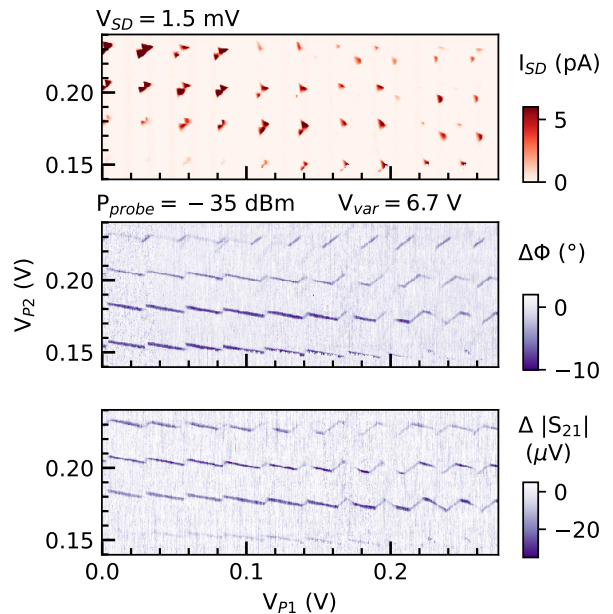


FIG. 8. **Dispersive charge sensing over an extended plunger gate voltage range** a) DC-current measurement of the charge stability diagram in the investigated Ge/Si core/shell nanowire device. b) Reflected phase $\Delta\Phi$ and c) RF amplitude $\Delta|S_{21}|$ measured along with the DC data in a). Here, we used a comparably large RF power $P_{probe} = -35$ dBm, leading to significant power-broadening of the lead and interdot transitions and reducing the scan resolution requirements.

In Fig. 8 we present a larger scale charge-stability map of the Ge/Si core/shell nanowire DQD. We note that these data were taken at the same barrier gate voltages as the bias triangles presented in the main text. The DC-current signal shown in Fig. 8 a) exhibits multiple bias triangles, corresponding to transport in a double quantum dot (DQD). Towards the upper right quadrant of the graph, there is a region with signatures typical for a triple quantum dot (TQD) system, where the electrochemical potential of the center quantum dot is aligned with that of one of its adjacent outer quantum dots [59]. The presence of both types of transport signatures in this configuration is an indicator for cotunneling involving the center quantum dot, as was previously observed in similar Ge/Si core/shell nanowire devices [47].

To make the lead and interdot transition lines more visible in the reflected signal, we increase the RF power to $P_{probe} = -35$ dBm, which significantly broadens the transitions in the scan. In this specific charge stability diagram, we observe strong lead transitions at the regions where the DC transport signatures are those of a DQD, whereas the interdot transitions are more pronounced in

the TQD region, indicating a change in the sensed quantum dot tunnel rates.

2. Tuning the interdot tunnel rate

The strength of the charge sensing signal is dependent on the tunnel rates of the sensed charge transition. To illustrate this, we show series of charge stability maps in Fig. 9, tracking a particular interdot transition at $V_{SD} = 0$ mV for different center barrier gate voltages V_{B2} . As the voltage applied to the center gate is reduced, the measured interdot transition becomes more faint, until it fully vanishes at $V_{B2} = 1.79$ V. The reduction in barrier voltage exponentially lowers the tunnel barrier, increasing the tunnel rate out of the sensitivity-window of our sensor [26].

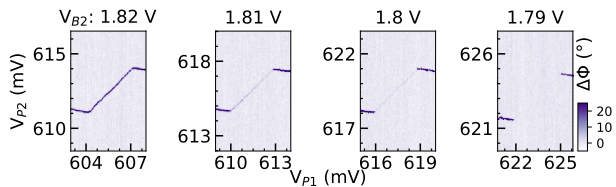


FIG. 9. **Dependence on the center barrier gate voltage V_{B2}** The strength of the reflected phase response $\Delta\Phi$ at the interdot line strongly changes within tens of mV applied to V_{B2} .

3. Reducing the lockin TC

In Fig. 4 of the main text, we have determined the SNR for the lead and interdot transition of a selected bias triangle as a function of the integration time t_{int} . We plot the closeup of an interdot transition and adjacent lead transitions at varying TC in Fig. 10 to illustrate the possible measurement speedup. As TC is decreased, the background noise increases, such that at $TC = 1.33$ μ s the transitions are barely visible anymore.

Appendix E: Charge-transition lineshape

Investigating the lineshape and linewidth of charge transitions, we can extract several quantum dot parameters. In the case of primarily dispersive signals, i.e. the transition manifests predominantly as a phase shift $\Delta\Phi$, we can model the signal as a capacitive correction to C_p , the quantum capacitance C_q . The dispersive shift $\Delta\Phi$ is translated to a change in circuit capacitance using the known slope $\frac{\delta\Phi}{\delta f}$ of $\Phi(f_{probe})$ at resonance for a given V_{var} and the well-known frequency-relation for a resonant tank circuit [57]:

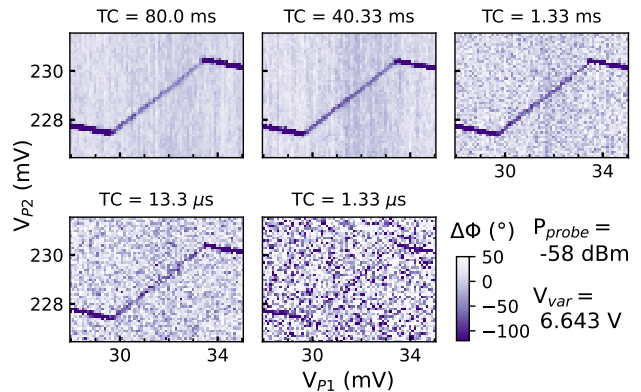


FIG. 10. **Dependence on the integration time** Interdot and lead transitions of a selected bias triangle, shown for varying TC . The signal can be recognized down to $TC = 1.33$ μ s.

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad (E1)$$

where f_{res} is the tank resonance frequency, L the inductance and C the capacitance of the resonator. The capacitive correction C_q is then:

$$C_q = \left(2\pi\sqrt{L}\Delta\Phi \cdot \frac{\delta\Phi}{\delta f} + \frac{1}{\sqrt{C}} \right)^{-2} - C \quad (E2)$$

In the following, we present the results of lineshape investigations of the lead transition and the interdot transition used also for the SNR analysis in the main text.

1. Lead transition

Fitting the lead transition lineshape recorded at $V_{var} = 7$ V, we find temperature-broadening to be dominant, $k_B T_H > \hbar\gamma_L$, where k_B denotes Boltzmann's constant, T_H the hole temperature of the lead, \hbar the reduced Planck's constant and γ_L the lead-dot tunnel rate [57]. We fit the phase signal to:

$$\Delta\Phi = \Delta\Phi_{max} \cdot \text{cosh}^{-2} \left(\frac{\alpha_{P1}(V_{P1} - V_{P1_0})}{2k_B T_H} \right) \quad (E3)$$

Here, $\Delta\Phi_{max}$ is the amplitude of the phase response and V_{P1_0} the center of the peak along the V_{P1} axis [57].

The dependence of T_H and $\Delta\Phi_{max}$ on the applied RF power P_{probe} shown in Fig. 11 indicates power-broadening to set in above $P_{probe} = -60$ dBm. In the regime of flat T_H , we find $T_H \approx 520 \pm 20$ mK and $C_{q,L} = 266 \pm 8$ aF.

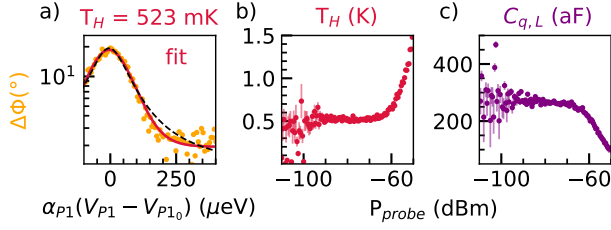


FIG. 11. **Fitting the lead transition lineshape** a) Example linecut (orange) of the lead transition recorded at $P_{probe} = -78$ dBm. The \cosh^{-2} fit (red) captures well the flank of the peak where a Lorentzian model (dashed black) fails. Note the logarithmic y-axis scale and zoom-in on the right flank of the transition to highlight the discrepancy between the two models. b) Fitted hole temperatures T_H as a function of probe power. c) Quantum capacitance of the lead transition $C_{q,L}$, calculated from the maximum phase shift at the charge transition. Power broadening causes a rise in the linewidth and reduced resonance height as observed for $P_{probe} > -60$ dBm.

2. Interdot transition

The dispersive signal at the interdot transition can be evaluated according to:

$$\Delta\Phi = \Phi_0 \cdot t_c^2 \left(\left(\frac{\alpha_{P1}(V_{P1} - V_{P1_0})}{2\sqrt{2}} \right)^2 + t_c^2 \right)^{-3/2} \quad (\text{E4})$$

Where the constant prefactor Φ_0 relates the term for the interdot quantum capacitance $C_{q,I}$ with the dispersive shift and t_c is the interdot tunnel coupling [57]. Note the additional factor $\sqrt{2}$ compared to [57], translating the quantum dot detuning axis into the plunger gate voltage axis.

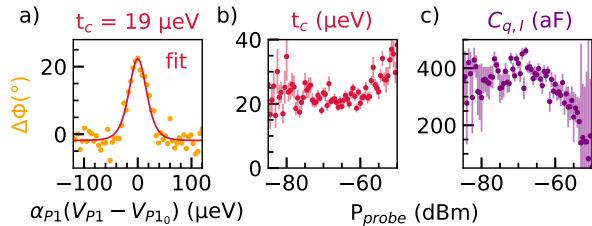


FIG. 12. **Fitting the interdot transition lineshape** a) Example linecut (orange) and fit (red) of the lead transition recorded at $P_{probe} = -66$ dBm. b) Fitted tunnel coupling t_c as a function of probe power. c) Quantum capacitance of the interdot transition $C_{q,I}$, calculated from the maximum phase shift at the charge transition. The signal is generally more unstable as compared to the lead transition, causing higher uncertainties.

The results of fitting an interdot transition-linecut as a function of P_{probe} are depicted in Fig. 12. In the regime

around $P_{probe} = -70$ dBm, $t_c \approx 22 \pm 5$ μeV and $C_{q,I} \approx 380 \pm 70$ aF are plateauing. Lower powers result in too low signal for reliable fitting while higher powers cause power broadening similar as in the case of the lead transition.

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