Chapter 2
GaAs Material and Crystal Properties—
A Tutorial

The motivation for using GaAs instead of silicon was summarized in Chapter 1. These advantages will be considered in more detail in this chapter, which serves as a tutorial review of GaAs material properties. Tutorial reviews have the advantage of presenting major elements of a topic without many detailed complexities. In doing so, there is danger of creating an impression of simplicity. We emphasize that GaAs materials technology began as almost a "black art," and has reached its present status through an enormous amount of scientific and technological development. Research in both crystal growth and epitaxial layer formation continues to be an active field of endeavor. Nevertheless, current technology adequately supports present production needs for GaAs wafers.

Gallium arsenide is a III–V compound semiconductor (it is composed of an element (Ga) from Column III of the periodic chart and an element (As) from Column V of the chart). GaAs was first created by Goldschmidt [1] in the 1920s. The first published article on the electronic properties of III–V compounds as semiconductors appeared in 1952 [2]. Since then, the importance of GaAs as a III–V semiconductor to both solid-state physics in general, and device physics in particular, has resulted in literally thousands of articles on this material. A 1982 review article on the intrinsic, major properties of GaAs [3], which intentionally omits any discussion of impurity phenomena or recombination phenomena, lists over four hundred references. Other reviews, some addressing the entire III–V family, are listed in references [4–11]. Further information may be found in the set of volumes from the Institute of Physics containing the proceedings of the biennial Conference on Gallium Arsenide and Related Compounds [12]. The series of yearly volumes titled, "Semiconductors and Semimetals" [13], also contains much information about GaAs.

Section 2.1 describes the advantages of GaAs. Section 2.2 reviews the physical and electrical properties of GaAs, including the troublesome determination of the dielectric constant. Section 2.3 reviews GaAs bulk crystal growth and individual

wafer preparation. Section 2.4 reivews the epitaxial methods used to grow active layers on GaAs substrates, including liquid phase epitaxy, vapor phase epitaxy, metal organic chemical vapor deposition, and molecular beam epitaxy. The latter two approaches are now the more popular, and variations on them will also be described. Section 2.5 describes the use of annealed ion implants to form active layers.

2.1 GENERAL CONCEPTS

Gallium arsenide has two principal advantages over silicon for microwave device use. First, its higher mobility and saturated drift velocity (discussed below) mean that electrons can move faster in GaAs than in silicon, and therefore devices can operate at higher frequencies. Second, GaAs can be readily produced in a semi-insulating substrate form. This semi-insulating substrate greatly reduces parasitic capacitances and allows the use of true monolithic integrated circuits operating at high speed (above 1 GHz). Other advantages of GaAs will be considered below.

The speed advantage is illustrated in Figure 2.1. When a carrier (electrons will be considered as the carriers for now) in a semiconductor is subjected to an electric field, it rapidly (about 10^{-12} seconds) achieves a velocity that is a function of the electric field strength. At low field strengths, this relationship is linear and the constant of proportionality is called the *mobility:*

$$v = \mu E$$

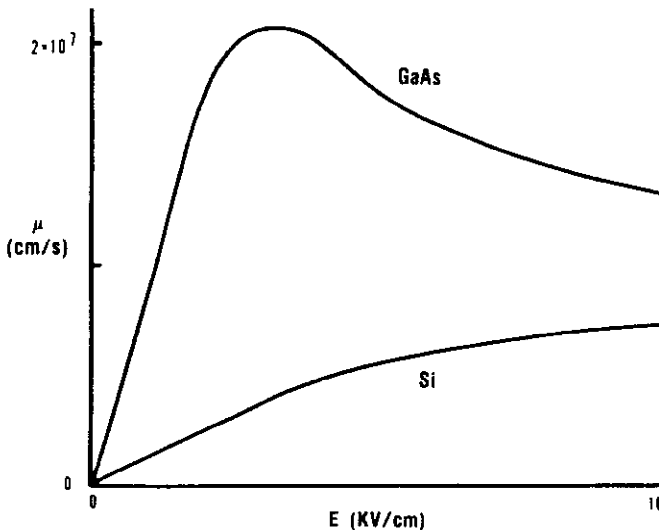


Figure 2.1 Drift velocity of electrons in GaAs and Si as a function of the electric field.

where v is the electron velocity (cm/s), E is the electric field strength (V/cm) and μ is the mobility and has units of cm^2/V-s. (Note that capital V is used for voltage; lowercase italic v is used for velocity.) This equilibrium velocity is the result of two opposing forces: the electric field, which tends to increase velocity; and electron scattering with the crystal lattice, which tends to limit the velocity. The scattering time is on the order of 10^{-13} seconds. However, as electric field strength continues to increase, the linear relationship no longer holds (Figure 2.1). The reasons have to do with the energy band structure of the semiconductor, and will be considered in the next section. The maximum velocity is called the *saturated drift velocity*. "Drift" velocities are those caused by electric fields as opposed to electron movement driven by concentration gradients (which are denoted as *diffusion*).

The electron mobility in the linear region is a function of temperature and impurity concentration (see Section 2.2), but is approximately six times greater for GaAs than for silicon. The maximum GaAs drift velocity is at least twice that of silicon for field strengths less than 2×10^4 V/cm. At typical field strengths, the advantage of GaAs may be much greater than a factor of two (Figure 2.1).

These advantages simply mean that appropriate GaAs devices and circuits can work at higher frequencies than silicon devices. The exact increase in speed depends on many factors. For example, comparable devices do not always exist in both media: MOSFETs (*metal oxide semiconductor field-effect transistors*) cannot be constructed on GaAs because of the lack of a suitable native oxide. Further, total speed for digital logic circuits also depends on the circuit capacitances that must be driven and the electric field regime in which the device operates (whether in the linear region or the saturated region). The consensus of several analyses [14–17] is that GaAs digital circuits should run two to five times faster than Si circuits, or have lower power dissipation. For analog applications, silicon transistors are hard-pressed to operate above 1 GHz. GaAs FETs work easily into the 20 GHz range and laboratory devices commonly are operated up to 60 GHz [18], with advanced device structures operating even higher.

The second major advantage of GaAs over silicon mentioned above was the availability of semi-insulating substrates. The bulk resistivity of materials (in general) extends from 10^{-6} Ω-cm to about 10^{22} Ω-cm, certainly one of the greatest ranges of any physical parameter. Semiconductors are in the range 10^{-2} to 10^9 Ω-cm [19]. Silicon generally can be made with resistivities of approximately 100 Ω-cm. GaAs, however, can be made with resistivities above 10^8 Ω-cm. This difference of resistivity of approximately six orders of magnitude means that, speaking colloquially, silicon substrates are not insulating, but GaAs substrates are. The active (current-carrying) GaAs for many devices consists of a thin layer on the surface of the semi-insulating substrate. Such a situation makes device isolation easy. More importantly, GaAs provides an ideal substrate on which to construct monolithic integrated circuits.

GaAs devices generally exhibit higher radiation hardness than do silicon devices (especially silicon MOS devices) [20], and hence are attractive for space and

military applications. The thin dielectric layers, such as silicon dioxide, used in the MOS devices makes them particularly sensitive to radiation.

The above characteristics mean that GaAs is preferred over silicon for high speed operation. Nevertheless, GaAs has some problems. First, it is much more susceptible to breakage than silicon. Dropping a GaAs wafer even a few inches onto a hard surface can result in breakage, or even totally shattering the wafer into small pieces. Thus, handling GaAs is more difficult than silicon. Careful attention to this problem in manufacturing environments, however, has essentially eliminated it as a major limitation. Second, GaAs does not have a stable native oxide that can "passivate" the wafer (see Section 2.2) in the manner that silicon dioxide does for silicon. This means that MOS devices that are a mainstay of silicon device technology cannot be used on GaAs. The dominant GaAs device is the *metal-semiconductor field-effect transistor* (MESFET) (see Chapter 3).

One final point should be made about the importance of GaAs. Unlike silicon, GaAs is a *direct band-gap* semiconductor (see Section 2.2), and so it is useful for fabricating optical components such as *light-emitting diodes* (LEDs) and lasers [8]. Although a discussion of such devices is beyond the scope of this book, the ability to fabricate those devices on the same substrate as other electronic circuitry opens the potentially vast field of integrated optoelectronics. Such work is actively being pursued in the laboratory.

2.2 PHYSICAL AND ELECTRICAL CHARACTERISTICS

The following subsections consider geometric and lattice properties, thermal properties, the dielectric constant, the energy band structure of GaAs, and electron and hole transport.

2.2.1 Geometric and Lattice Properties

The GaAs crystal is composed of two sublattices, each *face centered cubic* (fcc). The fcc structure is shown in Figure 2.2, and consists of atoms at the corners of a cube and also at the center of each face of the cube. The Ga atoms are arranged in such a pattern, as are the As atoms. These two sublattices are offset with respect to each other by half the diagonal of the fcc cube. Such a crystal configuration is called *cubic sphalerite* or "zincblende," and has the fcc translational symmetry. The unit cube for GaAs, showing the arrangement of Ga and As atoms, is shown in Figure 2.3. Each Ga (or As) atom has four neighbor As (or Ga) atoms. If the length of the unit cube is A (Figure 2.3), the bond length between these neighbors is $r_o = 3A/4$ and these bonds are separated by the tetrahedral bond angle of 109.47°. Undoped GaAs has a unit cell size at 300 K of [21]

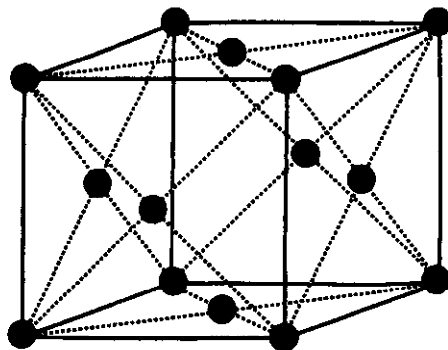


Figure 2.2 Face centered cubic (fcc) crystal structure: atoms are at the corners and in the middle of all faces of a cube. The gallium and arsenic atoms each form a fcc sublattice within the GaAs lattice.

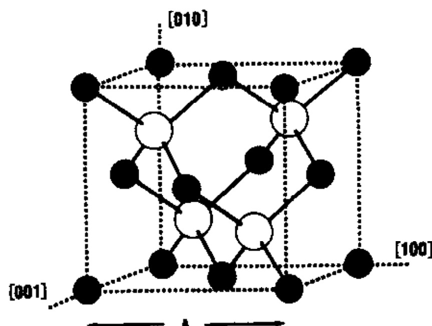


Figure 2.3 Unit cube of GaAs crystal lattice.

$$A = 5.65325 \pm 0.00002 \text{ Å}$$

and a density at 300 K of [22]

$$d = 5.3174 \pm 0.0026 \text{ g/cm}^3$$

A number of GaAs properties are contained in Table 2.1. The GaAs lattice constant A can increase up to 0.02% when a large concentration of a dopant is present [21]. Also, nonstoichiometric GaAs can result in slightly smaller values of A for As-rich GaAs, and slightly greater values for Ga-rich GaAs [22]. However, these variations in A are even less than the 0.02% mentioned above.

Figures 2.4 and 2.5 show truncations of the unit cube by specific planes within the crystal. A useful approach is to be able to speak of specific directions and planes

Table 2.1
Room Temperature (300 K) Properties of GaAs
(Discussed in the text and in Blakemore [3])

Property	Value
Lattice constant	5.65 Å
Density	5.317 g/cm^3
Atomic density	4.4279×10^{22} $atoms/cm^3$
Molecular weight	144.642 (69.720 + 74.922)
Bulk modulus	7.55×10^{11} dyn/cm^2
Shear modulus	3.26×10^{11} dyn/cm^2
Linear expansion coefficient	5.73×10^{-6} K^{-1}
Specific heat	0.327 J/g-K
Lattice thermal conductivity	0.55 W/cm-K
Dielectric constant	12.85
Band gap	1.423 eV
Threshold field	3.3 kV/cm
Peak drift velocity	2.1×10^7 cm/s
Electron mobility (undoped)	8500 cm^2/V-s
Hole mobility (undoped)	400 cm^3/V-s
Melting point	1238° C

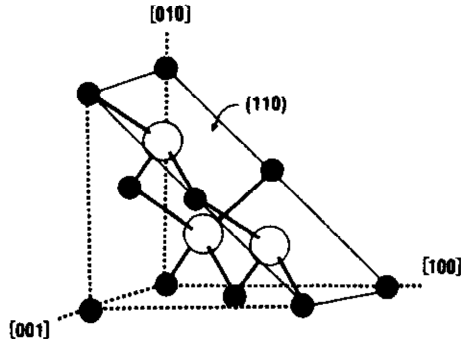


Figure 2.4 Truncation of the GaAs unit cube by the (110) plane.

within the crystal structure. *Miller indices* are used for this purpose, and consist of triplets corresponding to the three spatial directions. For example, the direction [110] may be conceived as a vector having components of $x = 1$, $y = 1$, and $z = 0$, where x, y, and z are oriented with respect to the unit cube (Figure 2.3). A negative direction is indicated by placing a bar over the index. Crystallographic planes are

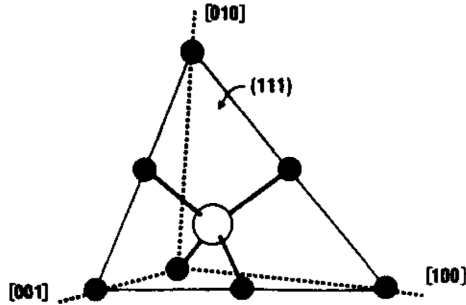


Figure 2.5 Truncation of the GaAs unit cube by the (111) plane.

designated by the direction normal to the plane's surface. Various types of brackets are used to enclose the indices; these have the following designations:

[•] indicates a direction: [111], [112], [100], *et cetera;*

(•) indicates a plane: (110), (101), *et cetera;*

⟨•⟩ indicates a family of directions (e.g., ⟨110⟩ represents directions [110], [101], [011]);

{•} indicates a family of planes.

Sometimes the above conventions are not rigorously followed, and the reader should beware of such instances.

Note that the {111} family of planes contains only one type of atom, either Ga or As. The letter A or B is attached to the plane to designate the Ga or As plane, respectively. Thus, of the eight planes contained in the {111} family, four are {111A} and contain only Ga atoms and four are {111B} and contain only As atoms. This distinction is important because the A and B planes have different chemical behavior and different growth (or etch) rates.

As we will discuss in subsequent sections, the most commonly used wafer orientation for GaAs device fabrication is (100). That means that the top surface of the wafer is a {100} surface. As shown in Figure 2.6, the two natural cleavage directions for such a wafer (along the (110) planes) are two perpendicular directions. Such GaAs wafers can easily be cleaved by using a diamond scribe to form a small scratch in either of the appropriate directions, and then using tweezers to "bend" the wafer apart at the scratch. With some experience, the wafer can even be cleaved (without using the tweezers) by applying heavier pressure with the scribe during the scratching operation. Figure 2.6 shows a (100) GaAs wafer with a raised mesa on its surface (produced either by localized growth, or by etching away other parts of the surface). Several crystal planes (facets) are exposed. Note that the {111B} surfaces (As planes) are smaller than the {111A} surfaces (Ga planes), indicating faster

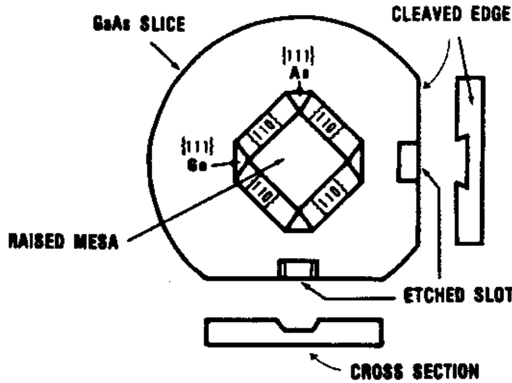


Figure 2.6 (100) oriented GaAs wafer illustrating cleavage planes and anisoptropy as evidenced by a raised mesa and etched slots.

growth (or slower etching) of the {111A} (Ga) planes. Figure 2.6 also shows profiles of an etched trough (using a common acid etch). Note that the profile is different for troughs oriented 90° apart. This lack of symmetry results from the interaction of etches with the GaAs crystal lattice. This is an important issue in device fabrication and is considered in detail in Chapter 5 (Wet Etching).

The crystal structure of GaAs will appear more dense when viewed in some directions than when viewed in others. This is illustrated in Figure 2.7, and has relevance for epitaxy and ion implantation, as will be discussed in the pertinent sections.

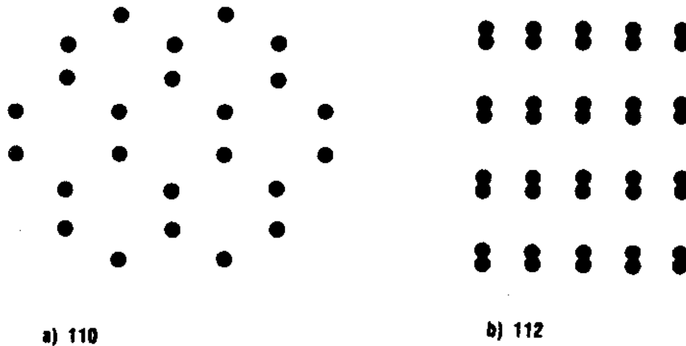


Figure 2.7 View of GaAs lattice from different directions: (a) along the [110] axis; (b) along the [112] axis.

2.2.2 Thermal Characteristics

The behavior of the coefficient of thermal expansion, α, (defined by $dL/dT = \alpha L$,

where L is length) of GaAs is a rather complicated matter when considered over a wide temperature range [11], especially less than 200 K or above 1000 K. Fortunately, such extremes are not relevant to general device processing and use. A number of investigators have published values for α at 300 K [22–27], the values ranging between $4.84 \times 10^{-6}\ T^{-1}$ and $6.9 \times 10^{-6}\ T^{-1}$. A quadratic approximation of the form $\alpha = A + BT - CT^2$ has been used to fit data from several of these investigations over moderate temperature ranges. A "consensus" polynomial was recommended [28] and, when modified slightly to adjust the balance point to 300 K (rather than 293 K in [28]), is given by [3]:

$$\alpha_T = 4.24 \times 10^{-6} + 5.82 \times 10^{-9}T - 2.82 \times 10^{-12}T^2\ \mathrm{K}^{-1}$$
$$\text{for } 200 < T < 1000\ \mathrm{K}$$

which gives a 300 K value of

$$\alpha_{300} = 5.73 \times 10^{-6}T^{-1}$$

(which is remarkably close to value of 5.7×10^{-6} quoted by the earliest of the abovementioned references [24]).

The coefficient of thermal conductivity, taken as equal to the lattice thermal conductivity, K_L, also exhibits complicated behavior over extreme temperature ranges, but is reasonably well behaved over more moderate temperature ranges [3, 29–32]. Figure 2.8 [3] illustrates measurements from several investigators over the approximate range of 200 K to 1000 K. The data show a general trend of decreasing thermal conductivity with increased doping. The 300 K value of K_L for undoped GaAs is approximately

$$K_L = 0.55\ W/\mathrm{cm\text{-}K}$$

Note that GaAs is a poor thermal conductor compared to silicon ($K_L = 1.5\ W/\mathrm{cm\text{-}K}$).

2.2.3 Dielectric Constant

Knowledge of the low frequency dielectric constant, K_o, is necessary for calculating parasitic capacitances, particularly for designing transmission lines on GaAs integrated circuits. (Low frequency in this case means below optical frequencies, and encompasses the frequency range of dc to 10^{11} Hz.) However, ascertaining the dielectric constant has not been as trivial as might be expected. As one reviewer stated [3], "One might reasonably expect this to be straightforward to the point of dullness. For GaAs, this has not been the case at all." The point is emphasized by considering

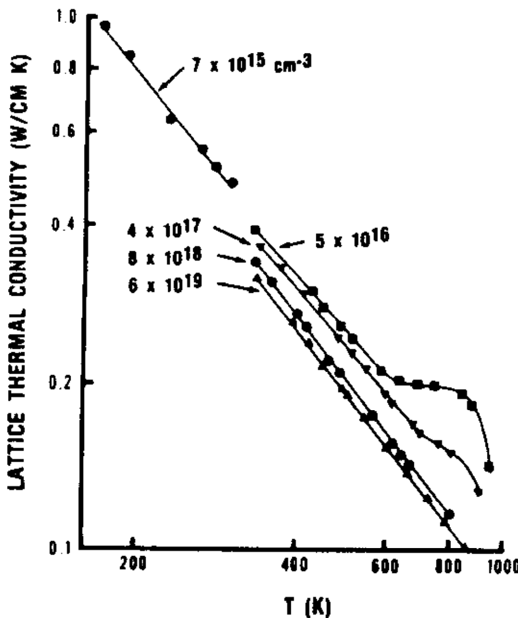


Figure 2.8 Lattice thermal conductivity (after Reference [3]; data from [30,32]). Note lower conductivity with increased doping.

the dozen or so room temperature measurements of K_o reported in one review article [33]. Even eliminating two anomalously low values left an unsatisfying range of 11.6 to 13.3 among the remaining measurements. That particular reviewer [33] recommended a choice of $K_o(300) = 12.9$, very close to the value of 12.91 chosen by another investigator [34]. More recent investigations have claimed $K_o(300) = 12.9 \pm 0.07$ for the range 4–18 GHz [35]. These and other measurements [36–38] were used by a recent reviewer [3] to recommend the expression:

$$K_o(T) = 12.4(1 + 1.2 \times 10^{-4}T)$$

which yields a 300 K value of 12.85. Therefore, we may reasonably take a 300 K value of

$$K_o(300) = 12.9$$

for three-digit accuracy. This is currently the commonly used value. Note that this value is significantly different from that of 12.5, which was published in 1961 [39] and used widely for some time therefore.

2.2.4 Energy Band Structure

An elementary understanding of the energy band structure of GaAs is necessary for properly understanding the transport properties (electron and hole current flow) in doped GaAs crystals. This section reviews the relevant information in a very simplified manner. A complete treatment of these matters may be found in reference [40]. The following discussion is intended for persons lacking a background in solid-state physics, and some oversimplifications are employed.

As is well known, electrons in isolated atoms can have only certain discrete energy values. This is the result of the laws of quantum mechanics. As individual atoms are brought closer together and assembled into a solid, the same physical laws result in electrons being restricted, not to single energy levels, but rather to broad bands of energies (Figure 2.9). The two bands of interest are called the *valance band* and the *conduction band*. They are separated by an energy gap (Figure 2.10(a) and (b)). At 0 K, all electrons are in the valance band and all its electron states are "filled." The laws of quantum mechanics do not allow two electrons to occupy the same energy state; hence, at 0 K, no electron movement is possible and the material is a perfect insulator. Above 0 K, some electrons have sufficient thermal energy to make a transition to the conduction band. Here they are free to move and can conduct current through the crystal. In the valance band, the absence of the electron is called a *hole* and can be treated as if it were a positive charge. These holes can move in the valance band and also can conduct current. In silicon, both types of carriers (electrons and holes) must generally be considered in device physics. In GaAs, how-

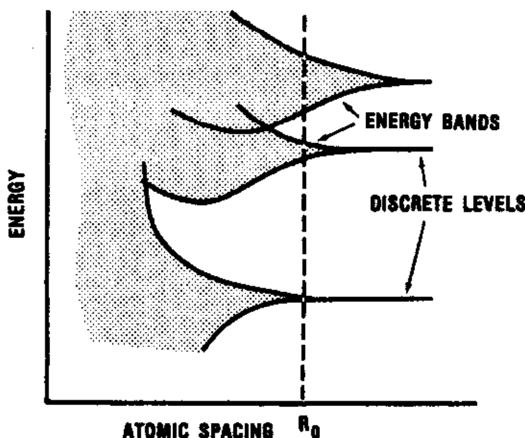


Figure 2.9 Energy band diagram showing creation of energy bands as discrete atoms assembled into a solid.

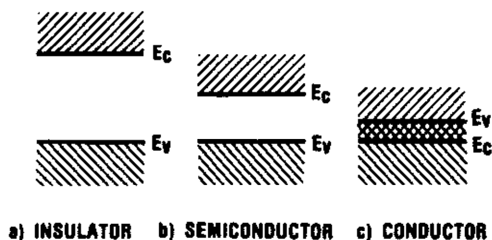


Figure 2.10 Band gap of three types of solids: (a) insulator; (b) semiconductor; (c) conductor.

ever, the hole mobility may be over an order of magnitude less than the electron mobility (see Section 2.2.5), and only the electron current need be considered in many GaAs devices. In this sense, then, such GaAs devices are *majority carrier* devices or unipolar devices.

The energy gap (between the valance and conduction bands) is an extremely important parameter. If it is large, few electrons will have enough thermal energy to reach the conduction band and the solid will be an insulator. Diamond has an energy gap greater than 5 eV and is a very good insulator. If the band gap is very small (or even nonexistent; i.e., overlapping bands), many electrons can reach the conduction band and the solid will be a conductor. The intermediate case is the semiconductor. These cases are illustrated in Figure 2.10. We noted in Section 2.1 that pure silicon is not as resistive as pure GaAs. This follows from their respective (room temperature) band gaps of 1.11 eV and 1.42 eV. However, actual material is neither absolutely pure nor perfectly crystalline; defects and impurities play a significant role in the resistivity of actual GaAs material (see Section 2.3).

A more complete band diagram for GaAs and for silicon is shown in Figure 2.11, which shows that the energy bands are functions of the magnitude of the electron (crystal) momentum. These relationships also depend on the crystallographic direction of the momentum, as indicated in the figure. GaAs is a "*direct band-gap*" semiconductor because the minima of the conduction band is directly over the maxima of the valance band. Transitions between bands generally involve movement from an energy state near the maximum of the lower band to an energy state near the minima of the upper band. Other transitions require greater energy and are less likely. In direct band-gap semiconductors, such a transition only requires a change in energy; no change in momentum is needed. Electrons can make this transition by emitting or absorbing a photon. This phenomena is essential to GaAs lasers and LEDs. Silicon, however, is an *indirect band-gap* semiconductor in that the minima and maxima of the two bands occur at different momenta. This means that for an electron to make a transition between bands, it generally must change momentum as well as energy, and hence must interact with the lattice (to change momentum). This is a much less likely thing to occur, and hence indirect band-gap semiconductors are not as suitable for optical devices such as lasers.

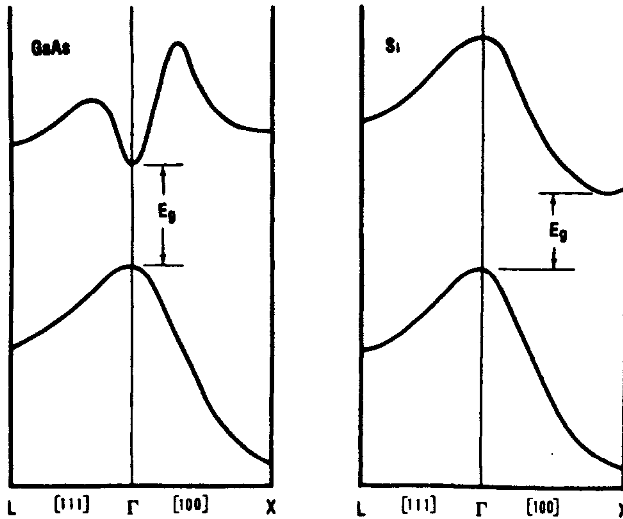


Figure 2.11 Energy band diagram of GaAs and silicon.

In all these cases, the term *band gap* refers to the energy difference between the minima and maxima of the conduction and valance band, even if they do not occur at the same momentum (Figure 2.11). The band gap is a function of temperature. For temperature below 1000 K, the GaAs band gap is accurately given by the expression [41]:

$$E(T) = 1.519 - 5.405 \times 10^{-4} T^2/(T + 204) \text{ eV}$$

which gives a room temperature value of

$$E(300) = 1.42 \text{ eV}$$

We also note that in the GaAs band diagram, minima in the conduction band other than the lowest one are present (Figure 2.11). If electrons have sufficient energy and interact (scatter) with the lattice, they can make transitions to these other minima or "valleys." This phenomenon is important in GaAs because it explains the decrease in electron velocity as the electric field in the crystal increases above a certain critical value (Figure 2.1). Electrons in these upper valleys would act as if their mass were greater than in the lower valleys [40]. Hence, their velocity is reduced after making such a transition. This phenomenon results in an apparent *negative resistivity* (an increase in electric field causing lower electron velocity) and is responsible for the *Gunn effect* in GaAs (see Chapter 3).

The energy band structure described above assumed a pure semiconductor and a crystal without defects or surfaces. Atoms were surrounded only by other atoms in the crystal. Any departure from this homogeneity, such as the presence of crystal defects, surfaces, or dopant atoms, changes the energy band structure near the inhomogeneity. In general, other energy levels then appear within the band gap of the semiconductor, as indicated in Figure 2.12. These levels are called *shallow* if they are near a band edge and *deep* if they are far from a band edge (Figure 2.12(a)). Figure 2.12(b) indicates the position of various energy levels within the band gap as caused by specific dopant atoms and defects.

Dopant atoms are intentionally introduced into the GaAs crystal structure to form conductive regions. These atoms are *n*-type dopants if they introduce extra electrons. In this case, the extra energy levels are near the conduction band and the electrons have enough thermal energy to make the small energy jump into the conduction band (Figure 2.12). Such atoms are often introduced either during epitaxial growth of the surface layers of the wafer (Section 2.4) or by ion implantation and anneal (Section 2.5). Of course, atoms are also unintentionally included in the crystal structure. To keep them out is virtually impossible. The nature of the problem is illustrated by noting that intentionally introduced dopant atoms often constitute only one part in 10^5 to 10^6 of the crystal atoms. Undesired impurities tend to dope the GaAs crystal, and hence decrease its resistivity. Consequently, chromium or oxygen is sometimes introduced into the crystal to compensate such doping and render the material semi-insulating (see section 2.3).

Crystal defects can introduce intraband-gap levels. These undesired levels are also called electron *traps* because they can trap electrons if they are far from the band edge. Such traps can increase the resistivity of the material. The general question of the number and cause of electron traps in GaAs remains a subject of research and debate. The principal deep electron trap in GaAs is located 0.76 eV below the

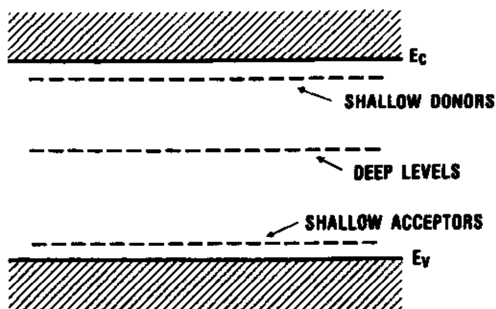


Figure 2.12 Energy states within the GaAs bandgap caused by impurity atoms or crystal defects: (a) generic; (b) specific levels.

conduction band edge, and is designated as EL2. It generally is believed to be related to the presence of an As atom on a Ga lattice site (the antisite defect AsGa), perhaps complexed with a neighboring vacancy [42, 43], although this is not yet certain. These traps will be discussed in greater detail in Section 2.3 on crystal growth.

Surfaces obviously represent locations where the lattice of atoms is discontinuous. Many other phenomena occur; in fact, surfaces are among the most complex topics in solid state physics. Various oxides are certainly present on GaAs (both of Ga and As), elemental arsenic may be present [39, 44], as well as numerous surface defects. These phenomena all cause extra electron states in the band gap, and are called *surface states*. In the case of silicon, the native oxide (silicon dioxide) is very effective in *passivating* these surface states. Generally speaking, the silicon dioxide acts enough like the native silicon that the Si to SiO_2 boundary does not introduce large numbers of surface states. A low density of surface state is needed for proper operation of MOS devices. Unfortunately, there seems to be no equivalent dielectric that similarly passivates GaAs, in spite of intensive efforts to discover one [45–48]. (The generally deleterious nature of surface states is beyond the scope of this brief review.) Unfortunately, use of dielectric coatings on GaAs devices for environmental and scratch protection is also often called passivation, but it certainly is not so in the sense used above. It may also be denoted as glassivation, especially if silicon dioxide is used.

2.2.5 Electron and Hole Transport

As described above, current flow in many GaAs devices is through electron flow, rather than by holes. The hole mobility is over an order of magnitude less than the electron mobility. Each is a function of temperature and carrier (electron or hole) concentration. General reviews may be found in references [33, 34, 49].

A general clarification is in order before continuing the discussion of electron and hole mobility. There are at least two types of mobility: the *drift mobility*, μ_d, and the *Hall mobility* μ_H. The drift mobility is the quantity used in Section 2.1, and represents the response of the carrier to a driving electric field. The Hall mobility represents the response of the carrier to a driving magnetic field perpendicular to the electric field. This is the well known *Hall effect*, in which carriers moving in a solid under an electric field (in the x direction) are subjected to perpendicular magnetic field (in the y direction) and hence develop a velocity perpendicular to both (in the z direction). There are well known techniques for measuring each type of mobility (Chapter 17). In general, the two types are not equal. The details of this distinction may be found in reference [40]. For the temperatures and doping ranges generally found in GaAs devices, the two mobilities are not greatly different.

Figure 2.13, taken from reference [49], shows data [50–56] of Hall mobility of holes at 300 K as a function of the carrier (hole) concentration. Note that these

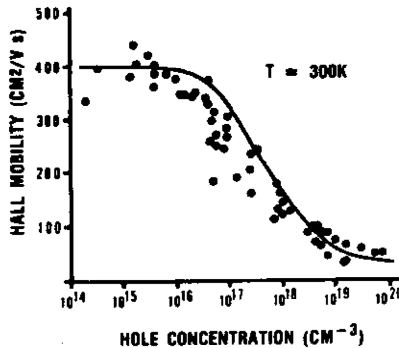


Figure 2.13 Hall mobility of holes in GaAs at 300 K as a function of hole concentration (after [49]; data from [50–56]).

values are generally below 400 cm^2/V-s, and substantially less than that for doping concentrations above 1×10^{17}.

Figure 2.14 shows similar data for electron mobility [57]. Note that for reasonable FET doping ranges (1×10^{17}) the mobility is about 4000 cm^2/V-s. The resistivity of GaAs that follows from these mobilities is shown in Figure 2.15 [40].

Figure 2.16, which shows electron velocity as a function of electric field is similar to Figure 2.1, except that it shows several sets of experimental data. The *threshold electric field*, E_t, is the value at which the velocity reaches the maximum. Doping inhomogeneities and other problems make difficult the measurement of E_t and the peak electron velocity to high accuracy. These values may be taken at room temperature (with 10% accuracy) as [3]:

$$E_t(300) = 3.3 \text{ kV/cm}$$

$$v_{max} = 2.1 \times 10^7 \text{ cm/s}$$

2.3 BULK CRYSTAL GROWTH AND WAFER GENERATION

GaAs is grown in crystalline blocks called *ingots* or *boules* and then individual wafers are sawed from the boule, lapped, and polished. There are two principal methods of growing GaAs bulk crystals: *horizontal Bridgman* (HB) and *liquid encapsulated Czochralski* (LEC). The two methods produce crystals having distinctive characteristics. Although LEC material has gained popularity as the method of choice for most GaAs work [58], the Bridgman method is still used also. Research is active in both types of material, and both show promise of continued improvement. We note that GaAs crystal growth remains as much technical art as science, and that the following discussion is only a general overview. Each of the two methods of growth (HB and LEC) have numerous variations; only the major approaches are described herein.

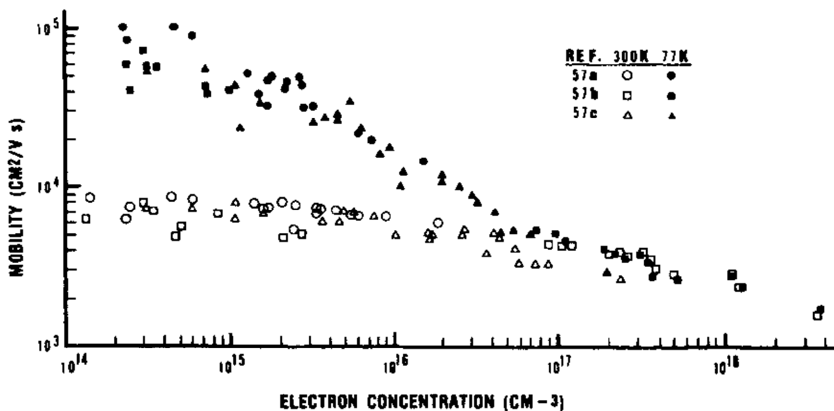


Figure 2.14 Electron mobility of GaAs at 300 K and 77 K as a function of carrier concentration [57].

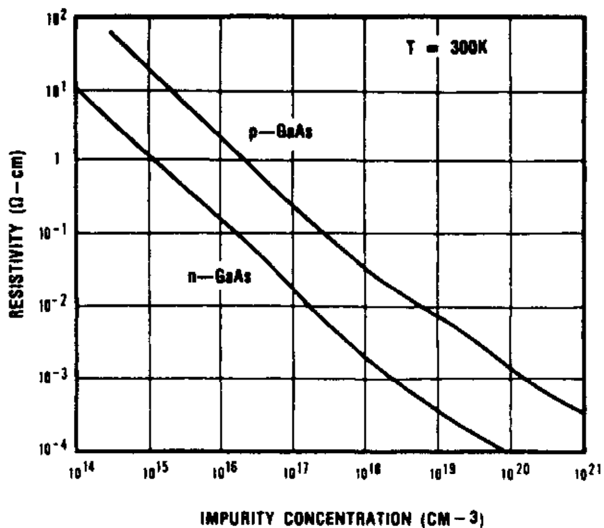


Figure 2.15 Resistivity of GaAs as a function of impurity concentration (after Sze [40]; data from S.M. Sze and J.C. Irvin, *Solid State Electron.*, **11**, 1968, p. 599.)

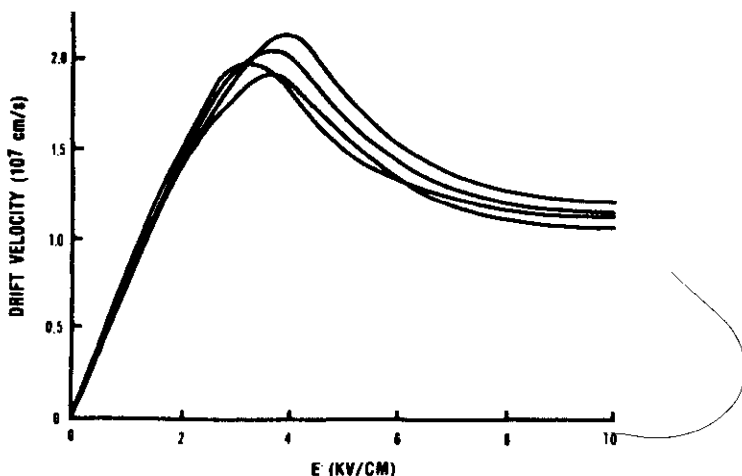


Figure 2.16 Drift velocity of conduction electrons in GaAs at 300 K as a function of electric field, experimental data (after [3]).

2.3.1 Horizontal Bridgman (HB)

In the horizontal Bridgman process, starting material (either pure gallium or polycrystalline GaAs) is placed in a long "boat" which is sealed in a quartz ampule several feet long. The ampoule is back-filled with an inert gas. A GaAs "seed" crystal is placed at the front of the boat and elemental arsenic is placed in the neck of the ampoule. This configuration is illustrated in Figure 2.17. Heating elements are used to generate a temperature profile in which the arsenic becomes gaseous, the gallium (or poly GaAs) is brought to the melting point of GaAs, and the seed region temperature is just below the GaAs solidification point. After the As has reacted with the Ga, either the ampoule or the heaters are slowly moved so that the temperature front moves along the length of the boat. Crystal growth then follows this temperature front. Growth is usually chosen to be in the $\langle 111 \rangle$ direction. This is a slow growth direction. Horizontal Bridgman material is sometimes called "boat grown" because of the use of the boat.

The completed crystal has a cross-sectional shape matching the shape of the boat, somewhat circular up to the level of the melt. If the crystal were sawed perpendicular to its axis, the resulting wafers would be (111) material. However, usually (100) wafers are desired, particularly for epitaxial growth reasons (see Section 2.4), and also for the desirable perpendicular cleavage planes of (100) material. For this reason, HB crystals are usually sawed at an angle of 54.7° to the ingot axis, and the resulting wafers are then (100). This angular sawing has one disadvantage: compositional variations along the axis of the crystal are converted into variations across individual wafers. The wafers generally have the shape shown in Figure 2.18 and

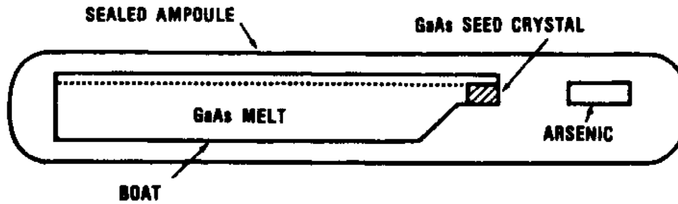


Figure 2.17 Schematic diagram of a horizontal Bridgman (HB) growth system.

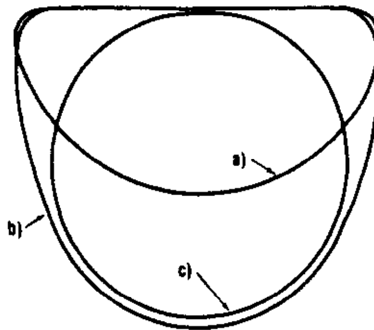


Figure 2.18 Shape of horizontal Bridgman wafers: (a) cut normal to crystal axis (111); (b) cut at 54.7° (100); (c) round wafer obtained from case (b).

are called "D-shaped" wafers. Note that the D-shaped material has a larger area than the cross section of the original ingot because of the angled sawing. Round wafers are required for true production operations, and this one trait makes D-shaped material undesirable. Such material may be made round by several methods. One is to cut each wafer in a round pattern. Another is to glue the D-shaped wafers together (surface to surface), and grind the resulting composite ingot round. Although the above operations may seem cumbersome, several vendors supply round HB material. Although D-shaped wafers were commonly used in earlier research and development work, they are rarely seen in today's more manufacturing-oriented environment.

The differences between HB and LEC material will be considered in the following discussion of the LEC technique.

2.3.2 Liquid Encapsulated Czochralski (LEC)

In the LEC process, the crystal is grown in the vertical direction by slowly pulling the boule from a melt (Figure 2.19). The melt consists of molten GaAs, and is confined by a layer of liquid boric oxide (B_2O_3) that floats on the surface of the

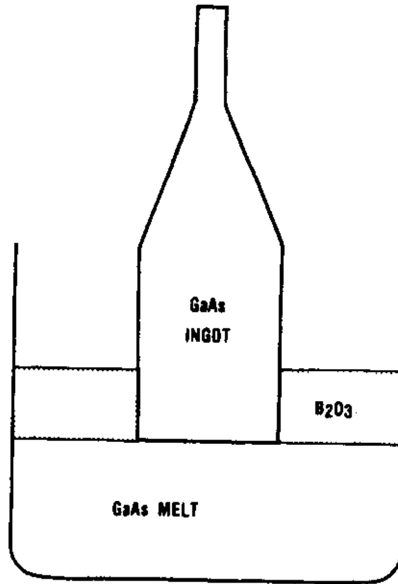


Figure 2.19 Liquid encapsulated Czochralski (LEC) growth of a GaAs crystal.

melt. The pioneering work of using the LEC process to grow semiconductor crystals, including the use of the boric oxide, was reported in 1962 [59]. Use of the technique to grow GaAs single crystals was reported in 1965 [60]. A GaAs seed crystal is used to begin the process, and appropriate temperature profiles are present. Growth is initiated by using the seed to penetrate the boric oxide and contact the melt. The melt is contained in a crucible. The seed and the crucible usually are rotated to reduce azimuthal thermal gradients. The diameter of the crystal is controlled by the pull rate and other operating parameters. The crystal growth machines used in this process are sometimes denoted as "pullers." The LEC process may be subdivided into low pressure LEC and high pressure LEC. The high pressure LEC process is performed under high ambient pressure (up to 50 atmospheres). Low pressure LEC is performed at about one atmosphere. The high pressure procedure was the original method, partly for complex historical reasons. Nonetheless, there seems to be no reason that the GaAs LEC process cannot be performed as well near ambient pressures, and several institutions have had great success [61]. The low pressure work, however, has generally required the use of different pullers. Changes in ambient pressure cause changes in the heat flow characteristics, and for this reason the high pressure machines cannot easily be used for the low pressure process without substantial modification. Low pressure machines are fundamentally smaller and less expensive. These seem likely to dominate in the future, but there are also experiments being performed at intermediate "medium pressure" conditions.

The GaAs melt must initially be prepared from exceedingly pure Ga and As. This process is called *compounding*. In the high pressure LEC pullers, the Ga and As are placed below the boric oxide, and the entire assembly is heated. The high ambient pressure over the boric oxide contains the rather violent reactions that occur as the Ga and As heat and react exothermally. Without such containment, local overheating would cause loss of arsenic and loss of control of the melt composition. The necessity for high pressure containment during compounding was a cogent argument for high pressure pullers; low pressure LEC required a "precompounding" operation in a separate machine. However, a successful technique for *in-situ* compounding in low pressure LEC pullers was developed, in which the Ga is first heated to the melting point of GaAs, with boric oxide floating on top. Then, the neck of a quartz ampule is inserted through the boric oxide into the gallium, and arsenic is added in a controlled manner [62]. This arsenic reacts immediately with the gallium until the melt is saturated. The low pressure *in-situ* compounding techniques gives improved control over stoichiometry (some amount of arsenic always escapes in the high pressure compounding operation). In either type of compounding operation, a desired impurity such as chromium can be placed in the crucible before compounding. Alternatively, if conductive substrates are desired, a dopant such as tellurium can be placed in the crucible.

The crucible which contains the melt is either quartz (SiO_2) or pyrolytic boron nitride (PBN). The quartz crucible adds more silicon to the melt than the PBN crucible. What is interesting is that quartz crucibles are used only once. They crack when the molten GaAs material is cooled at the conclusion of growth.

Bulk GaAs cannot be prepared in truly pure form. Remember that intentional doping may consist of only one atom for every 10^5 to 10^6 crystal atoms, and so we can easily appreciate the difficulty of lowering impurities to inconsequential amounts. Silicon is available from the quartz parts used in bulk growth. Carbon is available from graphite heaters, and may be transported in gaseous compounds. The ability to grow semi-insulating GaAs depends on complex compensation methods. Generally, shallow donors are compensated by deep acceptors (e.g., Si and Cr), or shallow acceptors are compensated by deep donors (e.g., C and EL2) [42]. If Cr is intentionally added (in the GaAs melt) to compensate silicon impurities, the material is said to be *Cr-doped*. This is generally required for LEC material grown from quartz crucibles, although the boric oxide tends to get some of the silicon. If PBN crucibles are used, the defect EL2 may serve to compensate impurities such as carbon. In this case, no dopant is added to the GaAs melt and the material is said to be *undoped*. Of course, it is undoped only in the sense that a dopant was not intentionally added. Chromium doped material is sometimes considered undesirable because Cr diffusion occurs during heating (such as following ion implantation). Chromium redistribution has been the subject of hundreds of papers over the years. The undesirable effects are not as severe in "lightly" doped Cr substrates (Cr concentration near 10^{15}). Such substrates can yield steeper doping profiles upon ion implantation, and have been used very successfully to fabricate many types of devices.

Chromium is generally used in quantities of about 0.1 to 0.3 ppma (parts per million, atomic). Higher amounts degrade the mobility of ion implanted material and decrease the activation [58] (Section 2.5). Chromium concentrations near the solid solubility limit (about 1 ppma) greatly increase the probability of crystal defects. Yet care must be taken, or this amount of Cr will not be sufficient to compensate the unintentionally incorporated dopants. The use of chromium has another drawback. Because it has a low distribution coefficient (6×10^{-4}), chromium concentration increases from seed to tail in LEC material and similar effects occur in HB material [58]. This difference can require different ion-implantation conditions for each wafer to maintain constant electrical properties. In fact, often desirable is to perform trial implants of two wafers from each new ingot (one near the seed end, one near the tail end) and to adjust accordingly the implant dose for the other wafers. For these reasons, undoped material is attractive for ion implantation. In fact, although Cr-doped material is still actively used, there is a general preference for undoped material, especially as its quality improves.

No crystal is perfect, and GaAs crystals have many dislocations in spite of the efforts to improve quality. These dislocations have deleterious effects. Dislocations introduce trapping states in the band gap, alter the etching properties of the wafer, but, most importantly, can alter electrical performance of devices. Exactly how this occurs is still under investigation, but what seems likely is that dislocations affect the activation of ion-implanted species. Studies have provided rather dramatic evidence showing that source-drain current and threshold voltage of logic FETs are strongly correlated with dislocation density [63]. Other work has shown that the threshold voltage of such logic FETs is affected, even up to distances of 50 μm from a dislocation [64]. As has also been demonstrated, sheet resistance and carrier concentration correlate closely with dislocation density [65]. In general, LEC material exhibits a greater dislocation density than HB material, and this is its major disadvantage compared to HB. Dislocation density depends strongly on the size ingot being grown. Small crystals can be virtually dislocation-free. There is also substantial scatter in the values obtained from crystal to crystal. LEC dislocation densities can easily be 10^4 to 10^5 cm^{-2} for two-inch or three-inch material. Comparable HB material generally exhibits lower dislocation densities, ranging from 8000 to 25,000 cm^{-2}. These are values that can be produced routinely; significantly better values can be produced. Also likely is that the evolving technology will steadily produce better material. *Dislocation density* can be determined by etching the wafer in hot KOH (about 400° C, 30 minutes), which preferentially etches at dislocations, and then counting the etched pits. Hence, the terms "dislocation density" and "etch pit density" are sometimes used interchangeably.

Dislocations generally arise from temperature gradients present during crystal growth. These are difficult to control. To reduce both axial and radial temperature gradients to a minimum is desirable. One effort, using thick boric oxide layers to reduce thermal gradients, has reported the case of 5000 dislocations cm^{-2} for two-

inch material, equaling the best results for HB [58]. There is reason to believe that future work will lower the dislocation densities that can routinely be obtained in three-inch LEC material.

Because of the radial nonuniformities in temperature and growth kinetics, the dislocation density is not uniform over a wafer, but generally exhibits a "W" pattern across any diameter, as shown in Figure 2.20 [65]. As indicated above, the sheet resistance tends to follow the same pattern (Figure 2.20).

Round wafers with orienting "flats" are desired for production. For LEC material, the general procedure is as follows. The ingot is ground so that it is round and of the correct diameter. X-ray or etching methods are used to orient the crystal, and a flat is ground along one side to act as an orientation marker. Normally, a smaller "minor flat" is also ground. Then, the ingot is sawed into separate wafers. These wafers are lapped on both sides and polished on either one or both sides. The completed wafers are generally 0.015–0.035 thick, and appear as shown in Figure 2.21. These substrates are then ready for ion implantation or epitaxial growth. Manufacturing in 1990 commonly employs three-inch material, although some two-inch material is still in use, while four-inch material is already being grown and limited use has begun.

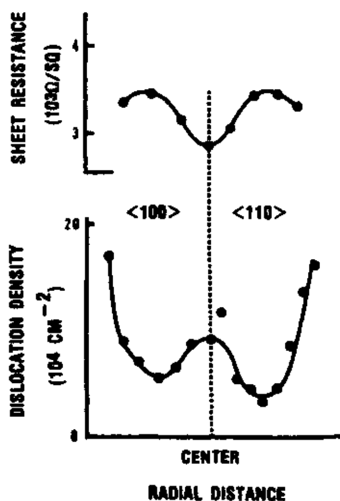


Figure 2.20 Sheet resistance and distribution of dislocations across any diameter of a round LEC wafer (after [65]). The "W" pattern of the dislocations is typical of LEC material.

2.4 EPITAXY

There are two methods of forming conductive GaAs surface layers on GaAs substrates: *epitaxy* and *ion implantation*. Ion implantation is considered in Section 2.5.

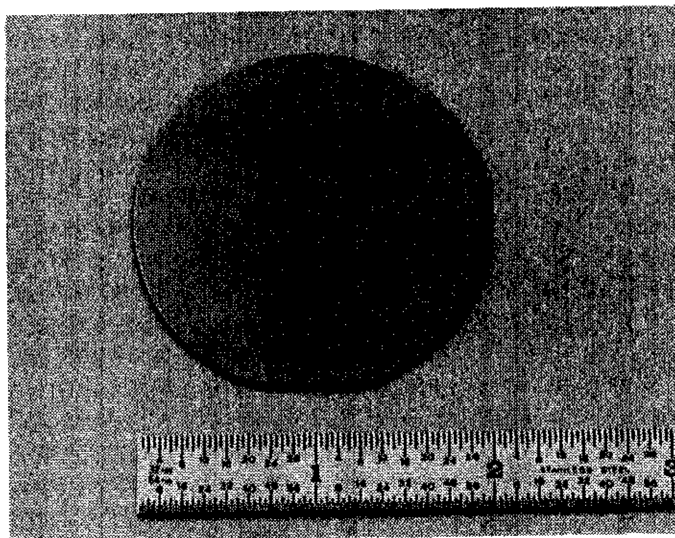


Figure 2.21 GaAs LEC wafer with flats.

Epitaxy consists of growing further GaAs material on the surface of GaAs substrates in a manner that preserves the crystal structure. Ga and As atoms are brought into contact with the crystal surface under temperatures, concentrations, and other conditions that result in crystalline growth. Dopants may be included among these atoms, and hence incorporated into the crystal on lattice sites. Epitaxial layers are generally of higher crystal quality than the substrate they are grown on. Although crystal defects tend to be preserved in the immediate overlaying epitaxial material, some "healing" does take place. If an active (doped) epitaxial layer is grown directly on the substrate, the impurities and defects in the substrate can degrade the crystalline properties, and therefore the electrical properties, of the epitaxial layer (these active layers may be only a few tenths of a micron thick). Therefore, "buffer" layers of undoped GaAs usually are epitaxially grown on the substrate before other, functional epitaxial layers are grown. Depending on the complexity of the device, the functional layers may consist of only one doped layer, or there could be a stack of many layers of different materials and dopant levels.

Epitaxial growth is generally performed on material that has been cut so that the crystal surface is slightly ($\approx 2°$) away from a $\langle 100 \rangle$ surface. This orientation results in the best morphology. For ion implantation, that misorientation is not necessary.

There are basically three types of epitaxy that have been used for GaAs: liquid phase epitaxy (LPE), vapor phase epitaxy (VPE), and molecular beam epitaxy (MBE), although each has many variations. The basic features of each will be described in the following subsections. The final subsection will address important variations of the basic techniques.

2.4.1 Liquid Phase Epitaxy

Liquid phase epitaxy is the oldest technique used to grow epitaxial layers on GaAs crystals. LPE was used in much of the early laboratory work. However, it is now rarely used because of limitations discussed below, and is virtually irrelevant for production of GaAs microwave devices. However, LPE remains an inexpensive method of epitaxy, and is capable of growing many material compositions including GaAlAs. Because of its relatively low cost, LPE is still found in university environments.

The LPE procedure is illustrated in Figure 2.22. A GaAs substrate is placed in a *slider* that can be moved across the surface of molten material contained in a boat. This material is gallium (or other materials) that has been saturated with the desired material (i.e., GaAs). The temperature profiles are such that the melt is supercooled just below its solidification point, and atoms solidify onto the crystal substrate. Dopants may be included in the melt. Different portions of the boat can contain different melts, so different compositions may be grown as the slider pulls the substrate across each zone. The major problem of LPE material is the difficulty of growing uniform layers over large surface areas.

We note that these objections refer to LPE material for microwave device application. LPE remains a successful production technique for LEDs and other such structures that do not require the thin, uniform, high quality epitaxial layers needed for microwave devices.

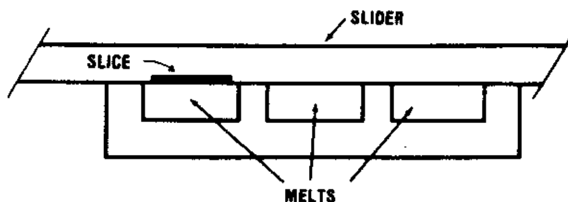


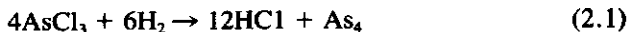
Figure 2.22 Schematic diagram of a liquid phase epitaxy (LPE) system.

2.4.2 Vapor Phase Epitaxy

Vapor phase epitaxy is one of the most used methods to grow epitaxial layers on GaAs substrates. In VPE growth, the Ga, As, and dopant atoms are brought to the wafer in a gaseous phase. Under appropriate temperatures and other conditions, reactions take place on the substrate surface that result in these atoms being deposited on the surface, where they replicate the underlying crystal structure.

Early work in VPE emphasized the $AsCl_3/Ga/H_2$ system. An $AsCl_3$ system was first reported in 1964 for growth of GaAsP [66]. Use of this technique for growing GaAs was reported the following year [67, 68]. The versatility of the system was improved by adding a second $AsCl_3$ bubbler [69] (see below). This became the main

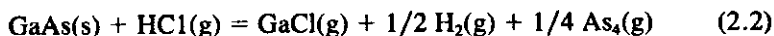
configuration of the system, and is shown in Figure 2.23. One or more wafers are placed in a quartz or graphite wafer holder within the reactor. The reactor is initially prepared by placing gallium in a boat near the front of the reactor tube. $AsCl_3$, which is a liquid, is placed in the "bubblers" shown in Figure 2.23. A major advantage of the $AsCl_3/Ga/H_2$ system was that the two starting materials (Ga and $AsCl_3$) may be obtained in very high purity. Before the reactor can be used for growth, a GaAs crust must be formed on the Ga metal in the boat. This is done by bubbling hydrogen gas through the liquid $AsCl_3$ and passing this gaseous flow over the gallium. The reactor is heated by ovens. Temperatures and gas flows are adjusted so that arsenic is made available to saturate the gallium under the reaction:



$$4AsCl_3 + 6H_2 \rightarrow 12HCl + As_4 \tag{2.1}$$

After a GaAs crust has completely formed over the Ga source, the reactor may be used for epitaxial growth. A limited number of growth runs may be accomplished before the source must be replenished.

For epitaxial growth, one or more wafers are placed in a quartz or graphite wafer holder in the reactor tube. The substrate may receive an *in-situ* etch before the growth process begins. Temperatures are adjusted so that the zone containing the gallium boat is hotter than the zone containing the substrate. The substrate zone is usually near 850° C. Hydrogen flows through the main bubbler and across the GaAs crust in the gallium boat. The exact reactions that occur are somewhat complex, but the process may be represented by the reaction



$$GaAs(s) + HCl(g) = GaCl(g) + 1/2\ H_2(g) + 1/4\ As_4(g) \tag{2.2}$$

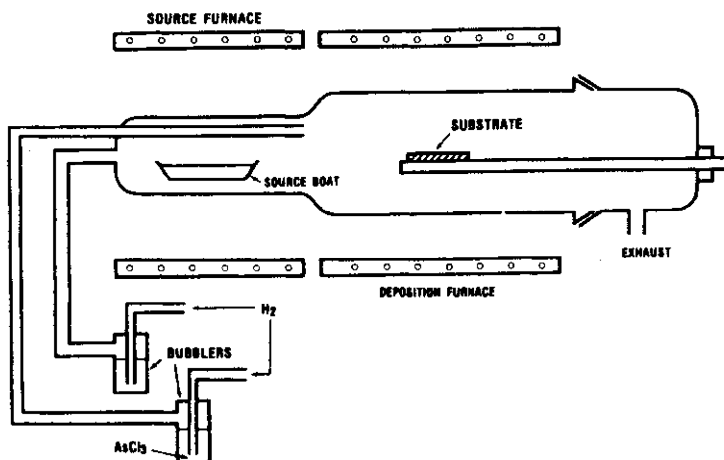


Figure 2.23 Schematic diagram of a vapor phase epitaxy (VPE) system.

where the letters s and g indicate either a solid or gaseous state. The reaction proceeds from left to right in the higher temperature zone over the source. The reverse reaction then occurs in the lower temperature zone at the substrate. The first bubbler is used for active layer growth. The second bubbler may be used in pregrowth etching or buffer layer growth. Dopants are introduced using another gaseous source such as H_2S for *n*-type doping.

A modification of the above procedure is to use high purity GaAs for the source instead of saturating a gallium melt. This is known as a "solid source," and the system is designated as $AsCl_3/GaAs/H_2$. The purity of the solid GaAs source (taken from bulk grown GaAs) is generally not as good as that which can be obtained by using the gallium saturation technique. Nevertheless, the purity seems adequate for many needs, and solid sources are used in many VPE systems.

Although the above system illustrates the fundamental principles of VPE, and is still used in some applications, another chemistry has become much more popular. The newer method involves transport of the gallium using organic molecules, and is designated MOCVD for *metal-organic chemical vapor deposition*. It is also sometimes referred to as *organo-metallic CVD* (OMCVD). Use of this method to grow III–V compounds was first reported in 1968 [70–72]. Trimethylgallium is often used as the source of gallium. Arsine (AsH_3), a highly poisonous gas, is used as the arsenic source. The advantage of MOCVD is its ability to grow AlGaAs layers; organic molecules such as trimethylaluminum work well in transporting Al, a requirement that has proven impossible using conventional (nonorganic) VPE. AlGaAs is an important constituent in some devices, as described in Chapter 3. These and other considerations have made MOCVD the dominant approach for vapor phase epitaxy, and a number of commercial firms manufacture growth reactors for MOCVD use. Still other commercial firms will grow epitaxial films to order using MOCVD. The major difficulty of the technique is the safety requirements and precautions associated with using arsine. Also, compositional and thickness uniformity across a wafer are not yet ideal, although certainly usable in production. Compositional uniformity tends to be better than thickness uniformity.

2.4.3 Molecular Beam Epitaxy

Molecular beam epitaxy is also a major method for epitaxial growth. MBE has significant advantages over MOCVD, but is more expensive. MBE may be described as a sophisticated evaporation technique performed in ultra high vacuum. In this procedure, the substrate is placed in a high vacuum and elemental species are evaporated from ovens and impinge upon the heated substrate. Here they assemble into crystalline order. With proper control of the sources (Ga, As, Al, Si, *et cetera*), almost any material composition and doping can be achieved. Further, the composition may be controlled with a resolution of virtually one atomic layer. Figure 2.24 shows a schematic view of the growth chamber of an MBE machine. The separate

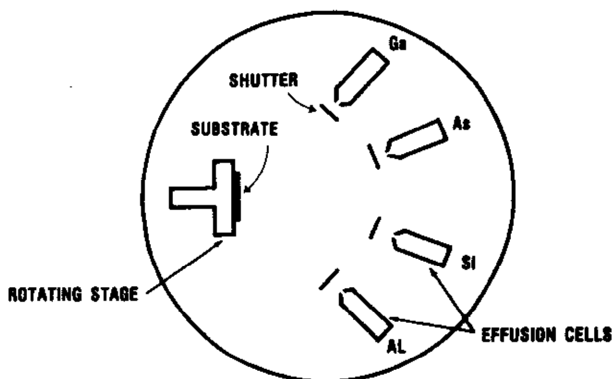


Figure 2.24 Schematic diagram of a molecular beam epitaxy (MBE) system.

ovens, often called *effusion cells*, each contain an individual element. The heated materials vaporize and exit the effusion cell through one end, go past a shutter, and travel through the growth chamber until reaching the substrate. More complex effusion cells, called *cracking furnaces*, can reduce molecular species to the dimmer form (e.g., As_4 to As_2). The substrate is heated to provide sufficient energy for surface diffusion and incorporation of the species. This temperature is typically 500° to 600° C for GaAs. The wafer is usually rotated to aid uniformity. Elements may be switched on and off by using the shutter in front of each effusion cell.

MBE's advantages are that it can produce almost any epitaxial layer composition, layer thickness, and doping, and can do so with high accuracy and uniformity across a wafer. Disadvantages include high vacuum requirements, complex and costly equipment, and slow growth rate. Ultra-high vacuum is required in the growth chamber, generally in the range 10^{-10} to 10^{-11} torr. This is an exceedingly difficult requirement, especially in the presence of heated substrates and heated effusion ovens. These require the presence of cooled shrouds and baffles to shield the heat sources. Hardly an understatement is to describe the design and construction of the growth chamber as a technological masterpiece.

Growth rate is typically 1 μm/h (about one atomic layer per second), although growth rates up to 10 μm/h may be attainable. As we may expect from difficult technology, cost is high. Yet MBE machines are available from several commercial vendors, and are in use in many laboratories. Some have wafer loading magazines so that several substrates may be simultaneously loaded into the vacuum system.

MBE machines usually incorporate instruments to analyze the growth process and the resulting crystal structure. The technique of *reflection high-energy electron diffraction* (RHEED) is generally employed for this evaluation. Such instruments may be in the growth chamber or in an adjacent chamber. Epitaxial layers grown

using MBE are more expensive than those grown by using MOCVD, although the technology is maturing rapidly, and this cost differential may decline. Several commercial firms offer MBE growth on three-inch wafers, and such wafers are being used in limited production environments.

Originally, scientists thought that MOCVD would be a much more manufacturable process than MBE (in terms of throughput and cost), and so would dominate in those applications where the superior MBE material is not absolutely required. However, the MBE equipment and processes have been maturing far more rapidly than the MOCVD equipment and processes in recent years, and which technology will eventually dominate is still uncertain.

2.4.4 Variations

The basic features of the two major epitaxial growth methods used in GaAs device production, MOCVD and MBE, were described in the previous two subsections. However, there are a number of variations of these methods that are actively being pursued in research environments. These may or may not prove permanently useful, but we ought to be aware of them. Major variations will be reviewed briefly in this subsection.

Migration enhanced epitaxy (MEE) or *migration enhanced MBE* (MEMBE) is a variation on the MBE process in which the group III and group IV atoms are sequentially deposited on the wafer by alternating the shutter openings on the Ga and As sources, for example. (In conventional MBE, both shutters are open at the same time and both types of atoms together impinge upon the wafer.) The intent is to give the group III atom some time to migrate over the wafer surface to yield a more perfect structure, possibly even at lower growth temperature. This technique is especially studied for growth of GaAs epitaxial layers on Si substrates.

Atomic layer epitaxy (ALE) is much like MEE, except that the emphasis is to form one atomic layer of each species at a time (so there is no real growth rate in the conventional sense). The potential advantage of this technique is based on the fact that the first atomic layer deposited is bound mainly by chemisorption, which is strong, while the second and subsequent atomic layers (of the same species) are bound by physisorption, which is less strong. By appropriately adjusting the growth temperature, the process is intended to be self-regulatory: one atomic layer will form, but not a second. This self-regulatory feature has obvious uniformity and compositional advantages. Further, the technique seems to have the ability to grow uniformly on sidewalls (of an etched trench, for example) in more complex applications. This approach is still mainly a research and development effort, and problems remain, but potential is high.

Another variation is to use the metal-organic sources commonly used in MOCVD in MBE. For example, triethylgallium may be used as the Ga source in the MBE

machine (and gases such as arsine and phosphine may be used as the group IV source). This variation is often called *metal-organic MBE* (MOMBE). Its major advantage is reducing the frequency and difficulty of replacing the material sources within the MBE machine. In conventional MBE, the machine must be opened to air and the effusion oven cooled to replenish material. This must be done rather often, and it is a slow process, which can require several initial runs to re-establish purity and control.

We noted above that a major problem in MOCVD is the safety requirements associated with the deadly gas arsine (a concentration of about 100 ppm can be lethal). So, there is interest in replacing arsine with other sources of As for MOCVD. There has been some success in these efforts, mainly involving materials such as *tertiarybutylarsine* (TBA). This material is a liquid (arsine is a gas, stored under high pressure) and is much safer to handle and to use. The ability of such alternative chemistries to produce acceptable epitaxial layers is actively being investigated. The ability to replace arsine would mean significant cost reduction by elimination of many of the extensive safety conditions and equipment currently associated with MOCVD.

There are also efforts in selectively growing epitaxial material on parts of wafers, rather than on the entire wafer. This technique is used for advanced circuity. The more common approach is to mask areas of the wafer with an oxide and to adjust growth conditions so that growth does not occur on the oxide. Other approaches use lasers to energize the growth reactions at the desired locations. Both approaches are not yet mature.

2.5 ION IMPLANTATION

Ion implantation at present is the most economical method to form active layers for production GaAs FET devices and MMICs, and is used extensively. Ion implantation is likely to remain popular and useful for a long time. In this procedure, dopant atoms are introduced into the substrate surface by ion implantation. Typical energies and doses are 30 keV to 400 keV and 10^{12} to 10^{14} atoms/cm^2. Such implantation greatly damages the crystal lattice, and the implanted atoms come to rest at random locations within the material. A high temperature annealing step (about 850° C) is performed to anneal out the lattice damage and allow the implanted atoms to move onto lattice sites. This is known as *activating* the implant. Not all the dopant atoms become incorporated at lattice sites and supply carriers. Activation is generally in the range of 75% to 95%, and depends on the implanting and annealing conditions.

Ion implantation has been an important element in silicon IC manufacture for some time, and so commercial ion implanters are readily available and implantation technology is well established. Ion implantation can be performed with high uniformity over a wafer and with good uniformity from wafer to wafer. Implantation