

## Title:

A shuttling-based two-qubit logic gate for linking distant silicon quantum processors

## Authors:

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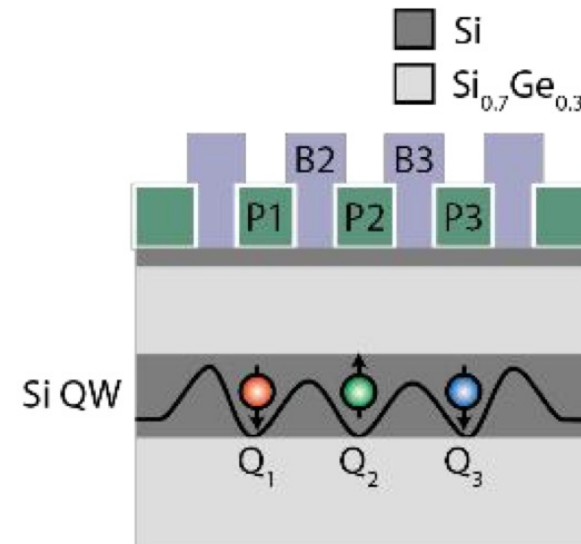
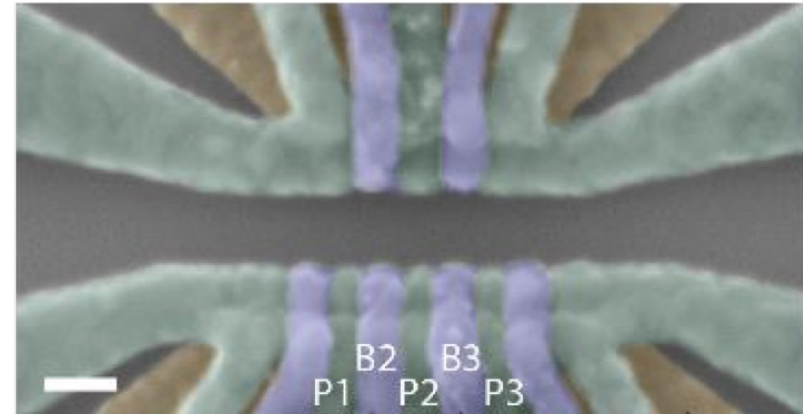
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**Fast universal quantum gate above the fault-tolerance threshold in silicon**

[Akito Noiri](#) , [Kenta Takeda](#), [Takashi Nakajima](#), [Takashi Kobayashi](#), [Amir Sammak](#), [Giordano Scappucci](#) & [Seigo Tarucha](#) 

# Device

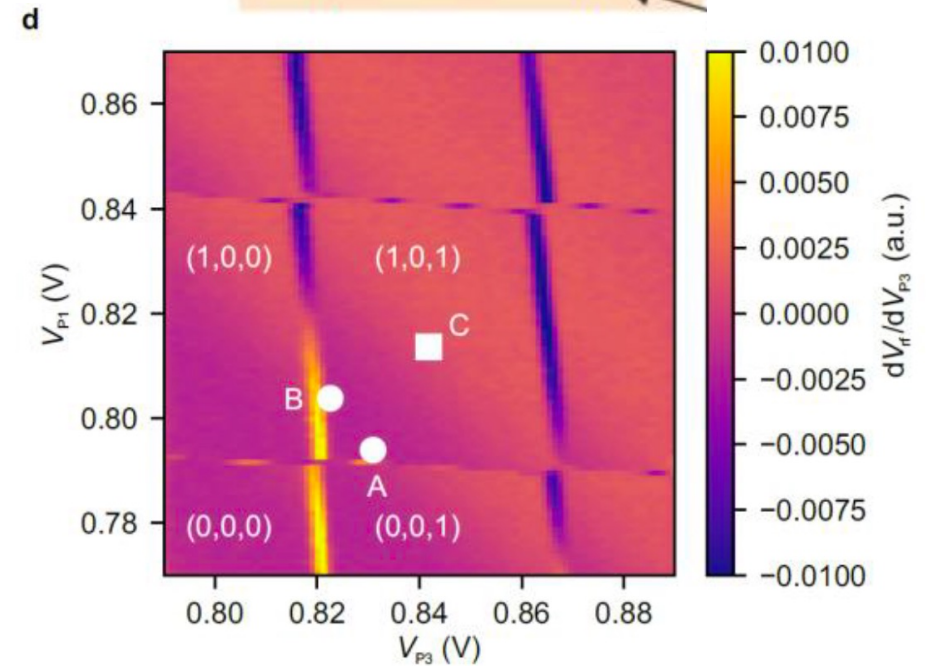
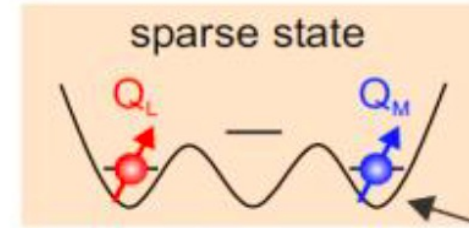
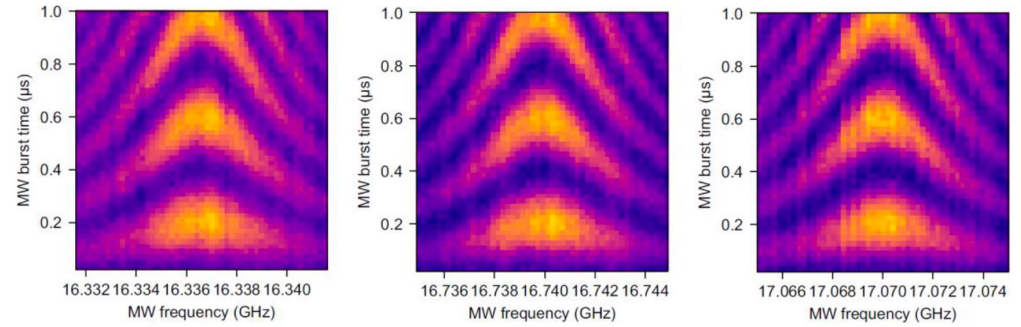
- Si/SiGe (QUTECH)
- 3 Al gate layers (Scr-Plg-Bar)
- Plunger : 65nm, Barrier : 25nm
- SET readout
- Can not tune exchange coupling with B gate (too thin)
- All Bs at 1V to allow coupling, above that hysteresis appears
- Essentially a Plunger-only device



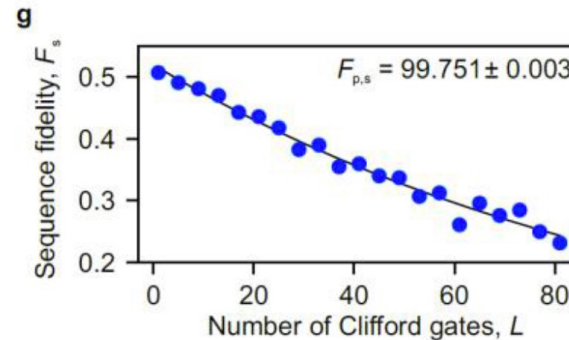
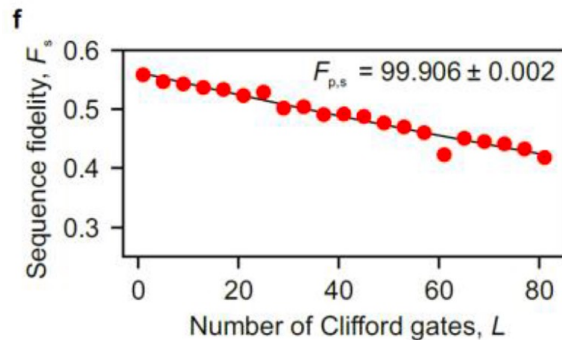
+ cobalt micromagnet (EDSR) -> DEz 403 MHz

# Sparse state

- 1 electrons on QD1 & QD3
- Initialization & Readout by energy selective spin tunneling with reservoirs (A & B)
- Not Virtual Gates CSD
- $T^* = 3$  &  $4$  us  $\rightarrow$  echo  $18$  &  $28$  us
- Simultaneous CRB  $\rightarrow$  both  $F_s > 99.7\%$

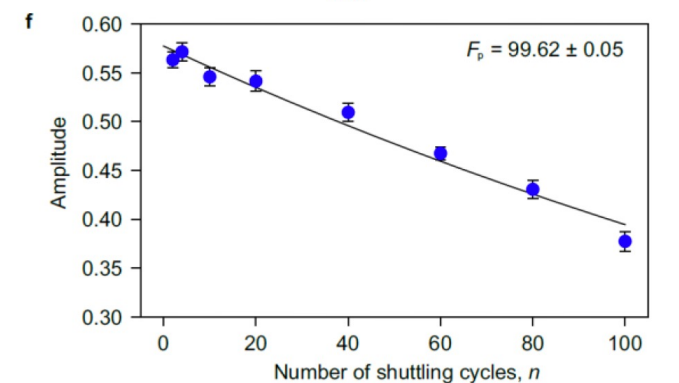
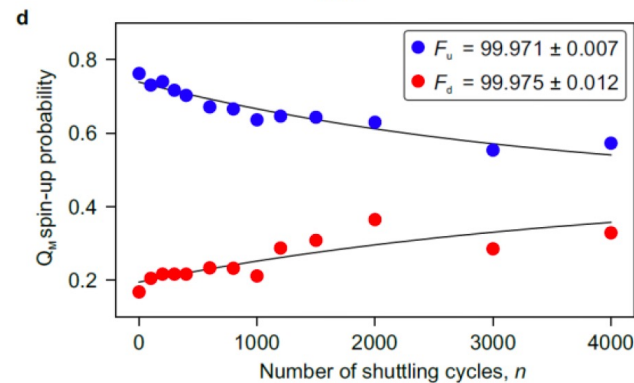
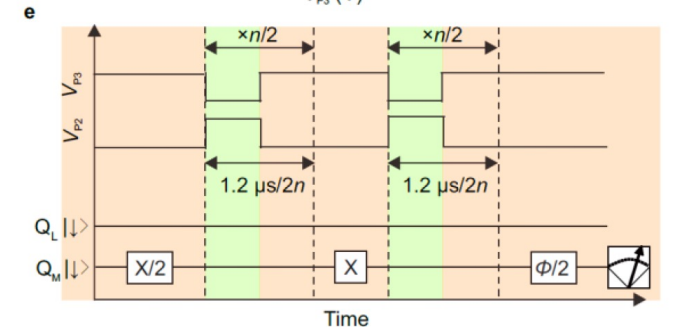
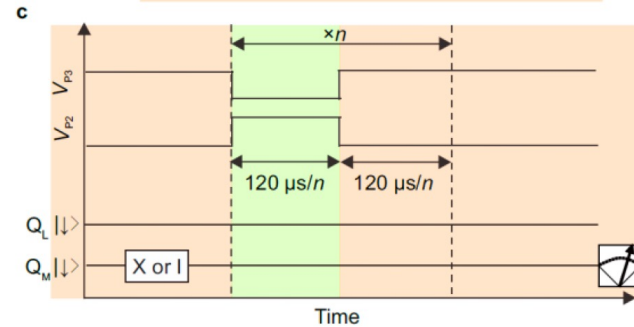
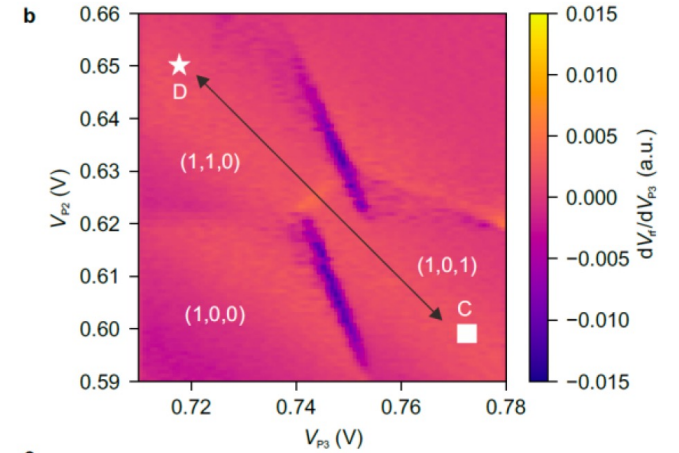
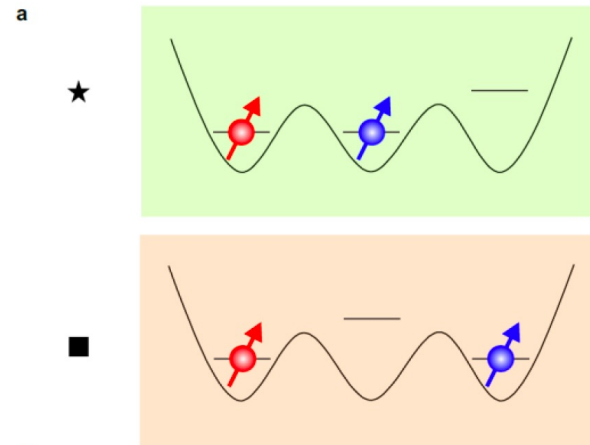


$$J = 0.89 \pm 0.10 \text{ kHz}$$

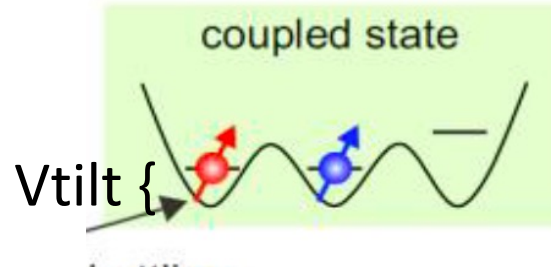


# Shuttling

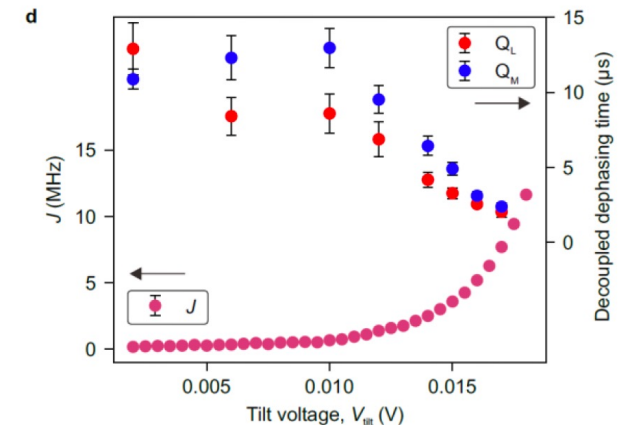
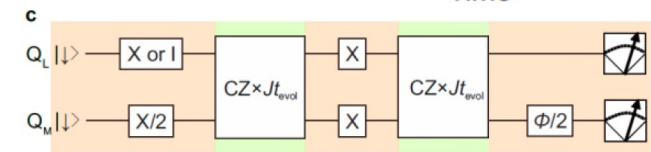
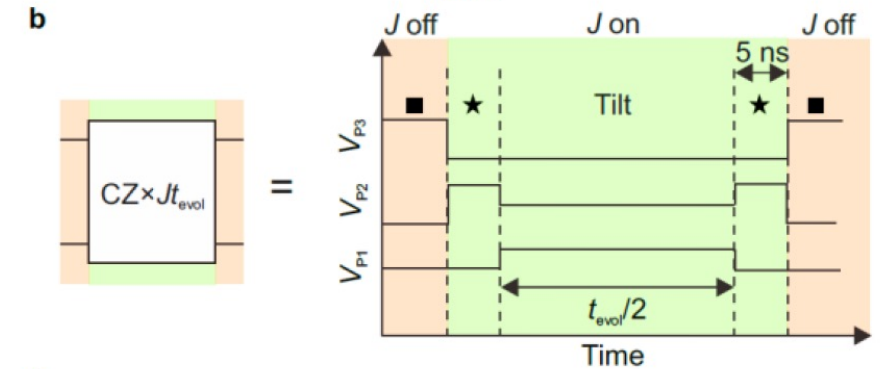
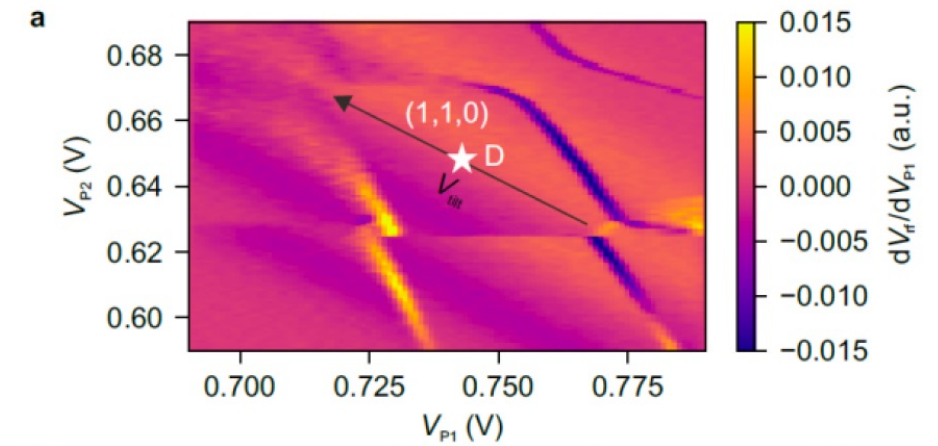
- Tright : 20.2 GHz
- Perform spin polarization fidelity estimation >99.95% p.c.
- Perform spin coherence fidelity estimation >99.5% p.c.
- MOS 99.97% & 99.4% (UNSW 2021)
- ~500 dots (~45  $\mu\text{m}$ ) before coherence  $1/e$ .
- Phase shifts (DEz) can be removed by a phase gate



# Shuttling Gate

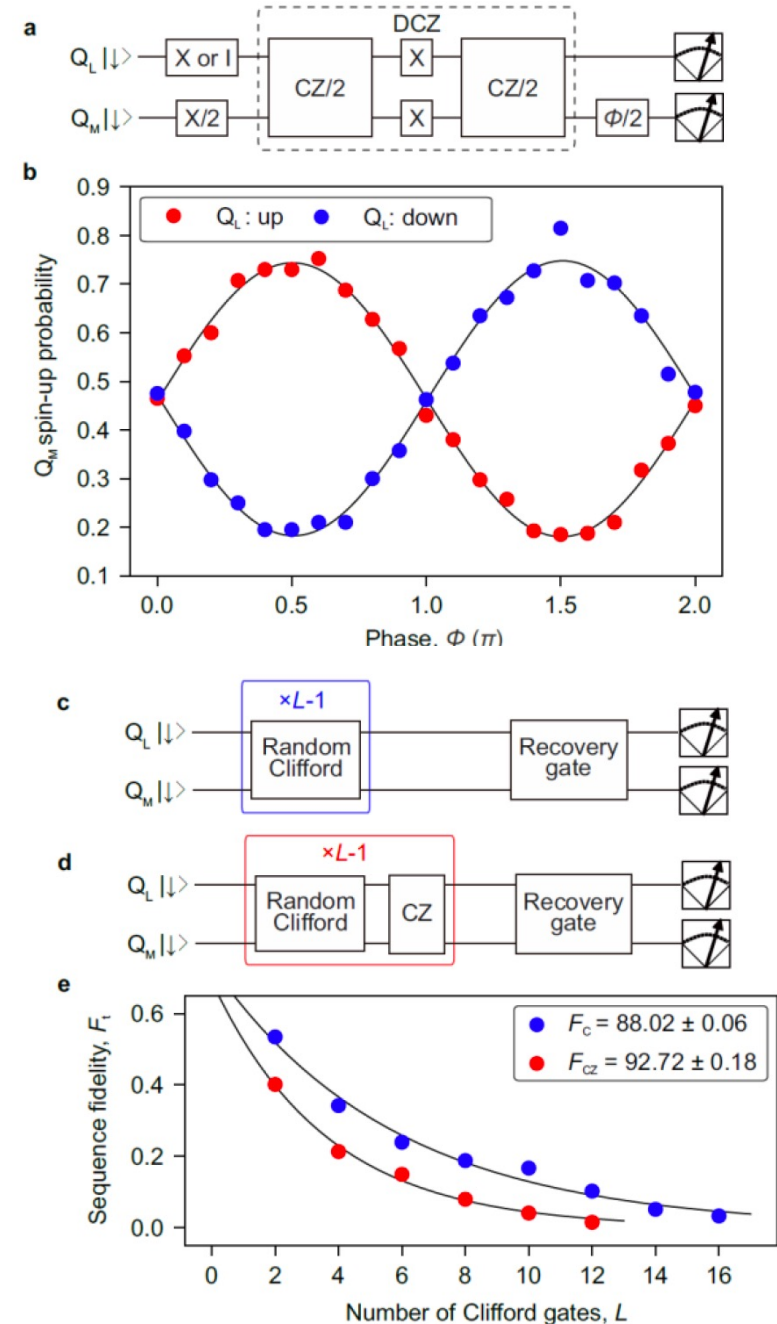


- $V_{\text{tilt}} \rightarrow$  detuning induced exchange interaction  $J$
- 5ns wait time to avoid charge transitions and no ramp time in pulse included
- Coherence drops –  $J$  increases with  $V_{\text{tilt}}$
- Optimum for CZ,  $V_{\text{tilt}}=0.012$  V with  $J=1.25$  MHz
- One thousand switching ratio of  $J$



# DCz shuttling gate

- $t_{\text{evol}} = 1/2J = 0.4 \mu\text{s}$
- Decoupled CZ (DCZ) gate to suppress low-f dephasing during the c-phase evolution (by half time pi pulse)
- The obtained controlled phase is  $1.003 \pm 0.01 \pi$
- CRB  $\rightarrow F_c > 88\%$ ,  $F_{cz} > 92.5\%$
- This is due to the slow  $t_{\text{evol}} = 0.4 \mu\text{s}$
- Faster gate with use of barrier gate would improve it



# Summary

- Successful implementation of shuttling gate
- Improvement of the turn-off of  $J$  between 2 Qubits ( $<1\text{kHz}$ )
- Low fidelity of CZ is due to absence of barrier tuning of  $J$
- High fidelity of shuttling coherence achieved