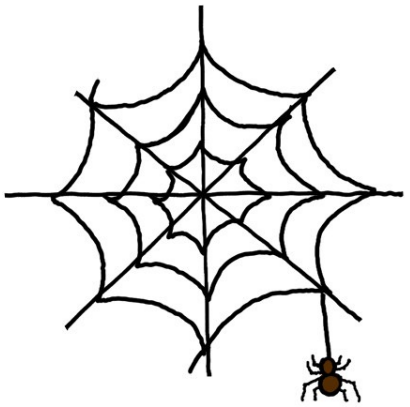

The *spider-web* array–a sparse spin qubit array

ASML UNSW

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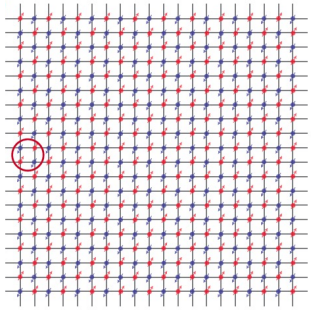
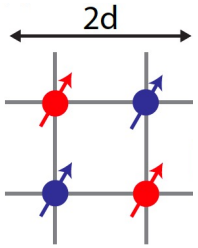
(Dated: October 4, 2021)

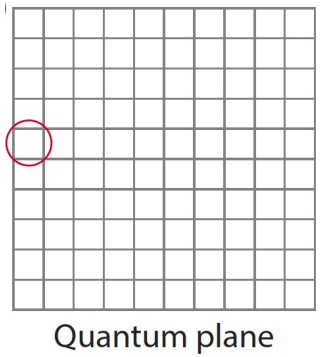
Contents

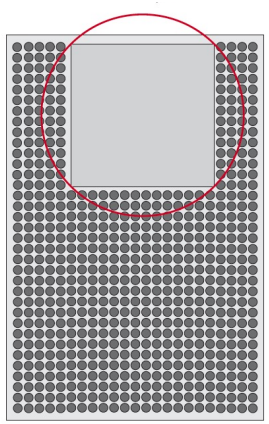
- Elements of the Sparse Array achitecture
- Operation principle and surface code implementation
- Integration of classical control electronics
- Footprint , line scaling & heat discipation (1Million Qbits example)

Array Design and Operation









Sparse Array Architecture:

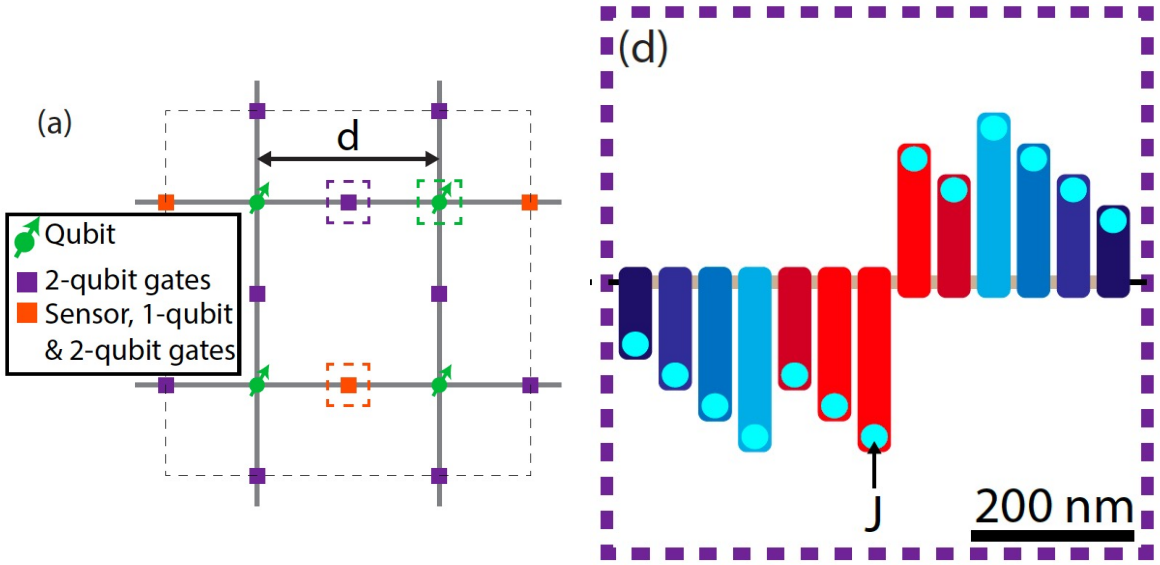
- Allows integration of control electronics (DC bias)
- Robust against inhomogeneities in the substrate
- Reduces crosstalk
- Requires coherent spin shuttling along um distances

Components:

- Unit cell → 4 (2 Data+2 Ancilla) Qubits → d=10um
- Module → common DC bias & Readout
- Space in final die for extra electronics

Unit Cell Operation

2 Qubit Gate Area

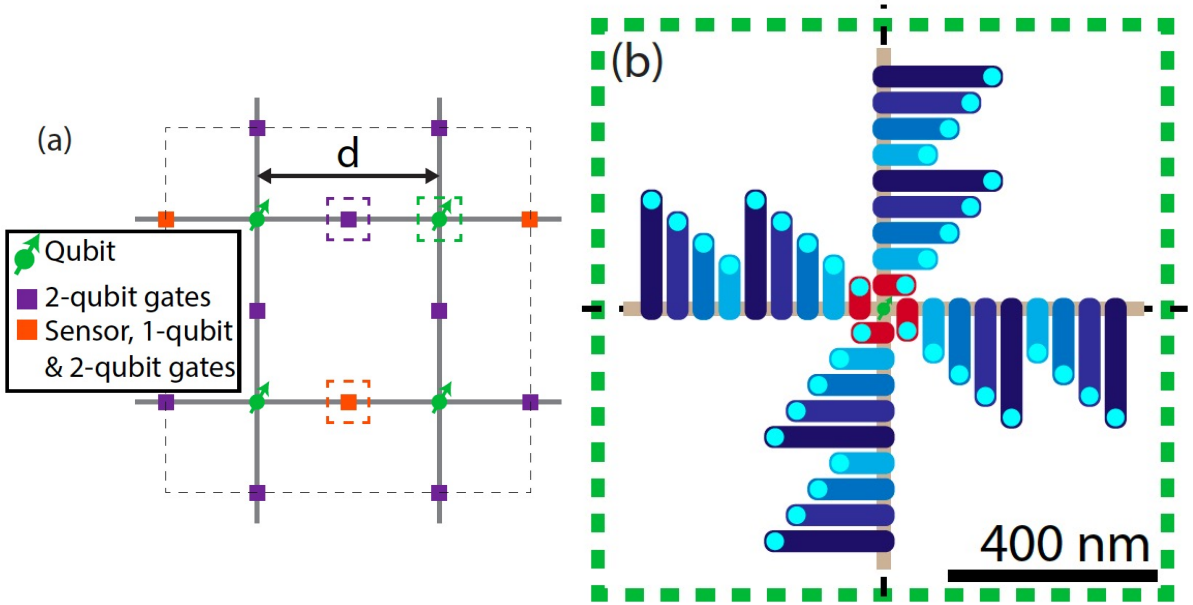


- 6 per unit cell
- 2 vertice gates (**red**) act both for confinment & tunneling to shuttling channel (C)
- 4 phase shifted signals at groups of 4 gates(**blue**) create travelling potential wave for shuttling (P)
- 2 plungers (for the spins) amd 1 exchange barrier gate J for 2 Qubit operations (fine)

Region	Regions in unit cell	Fine (1 µV)	Coarse (1 mV)	Pulsed gates
Two-qubit only	6	3	2	5

Unit Cell Operation

Idling Qubit Area

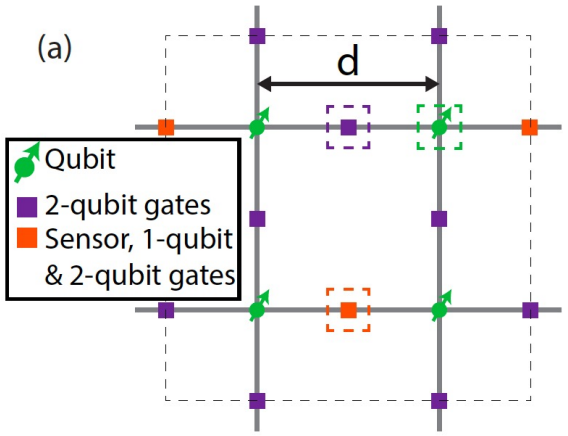


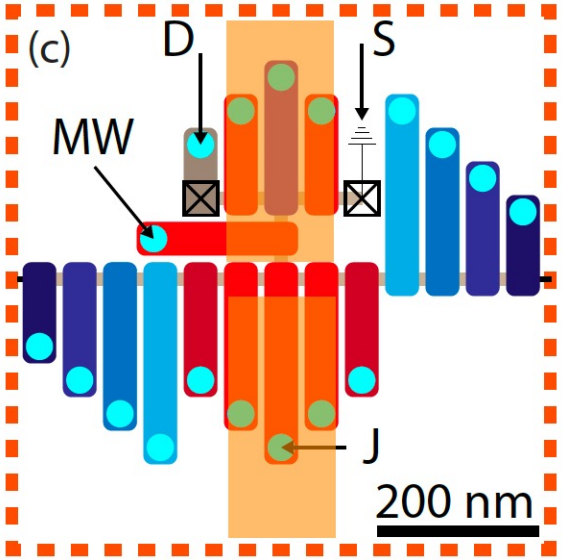
- 4 per unit cell
- 4 barrier gates (**red**) act both for confinment & tunneling to shuttling channel (C)
- 4 phase shifted signals at groups of 4 gates (**blue**) create travelling potential wave for shuttling (P)
- Shuttling gate do not require DC bias by using large potential amplitude to eliminate inhomogeneities

Region	Regions in unit cell	Fine (1 µV)	Coarse (1 mV)	Pulsed gates
Qubit idling	4	-	4	4

Unit Cell Operation

Readout, 1 & 2 Qubit Gates

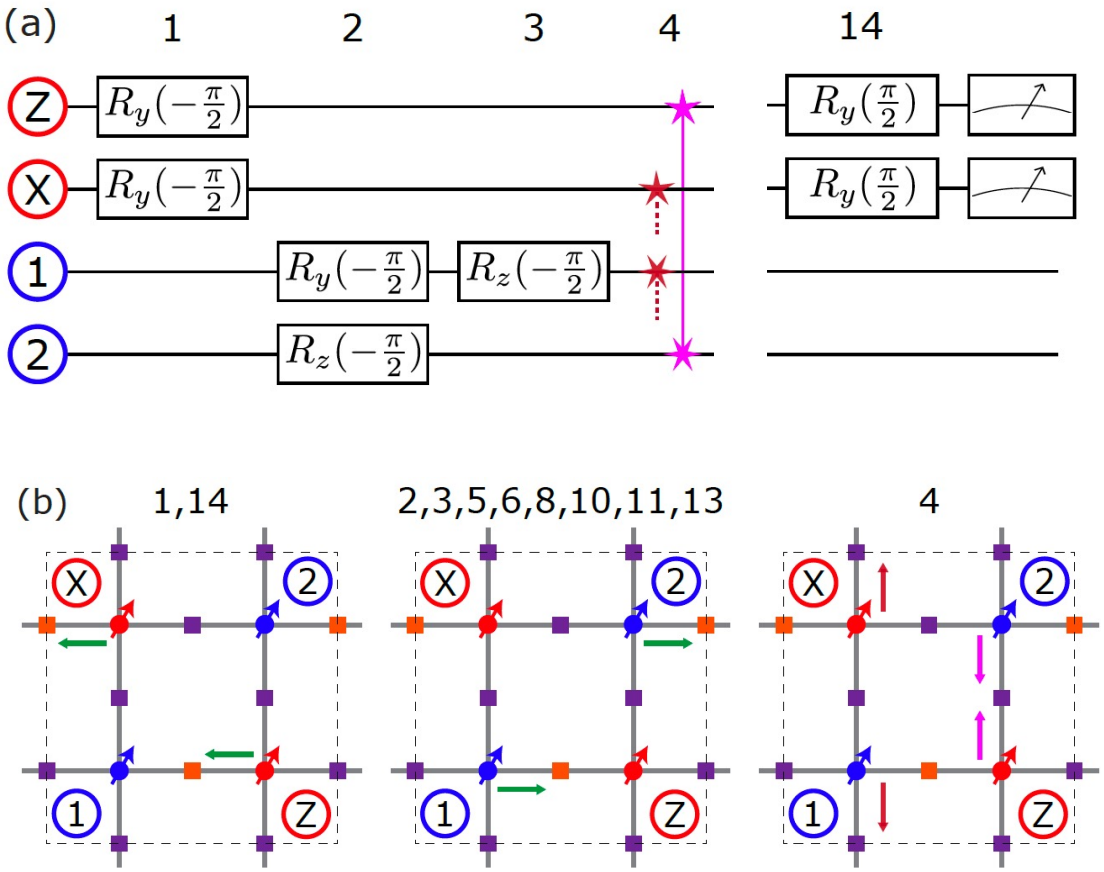




- 2 per unit cell
- 2 barrier gates (**red**) control tunneling to shuttling channel (C)
- 4 phase shifted signals at groups of 4 gates (**blue**) create travelling potential wave for shuttling (P)
- SET = 2 barriers (c)+ 1 plunger (C) + 2 Ohmics
- 1 Microwave line for driving single qubit gates
- 2 plungers (for the spins) amd 1 exchange barrier gate J for 2 Qubit operations (fine)

Region	Regions in unit cell	Fine (1 µV)	Coarse (1 mV)	Pulsed gates
Qubit operation	2	7	2	6

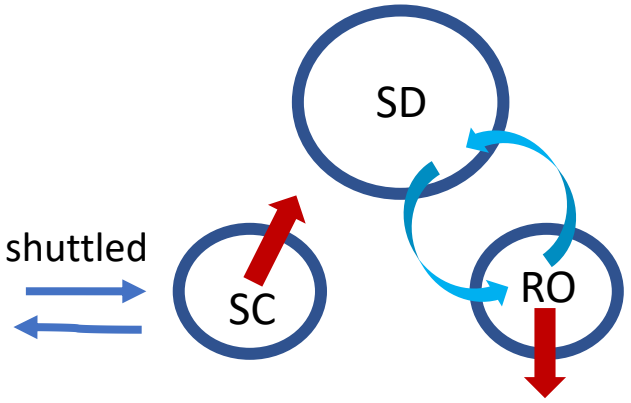
Example: Surface code cycle

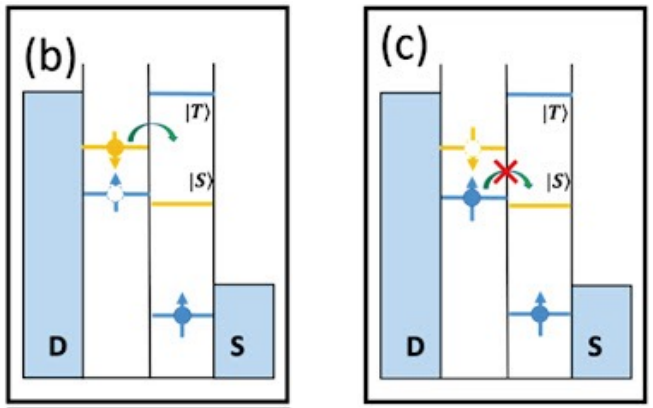


- Single Qubit rotations achieved by tuning EDSR microwave pulse
- Two Qubit gates achieved by the pulse applied to the J gate (SWAP based 3 step gate), (red purple stars)
- Readout only at the SC-ancilla qubits at the dedicated points
- Shuttling gate not require DC bias by using large V amplitude to eliminate inhomogeneities
- Time of cycle:

$$t_{sc} = 22\,t_{sh} + 14\,t_{1q} + 8\,t_{sw} + t_r$$

Readout





Protocol

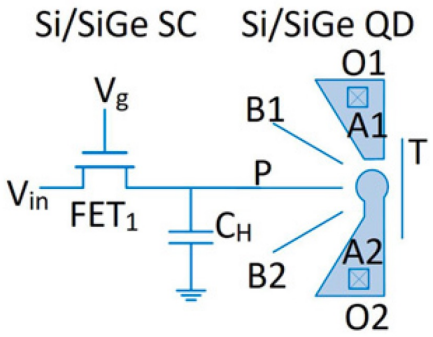
- PSB readout technique for higher T operation
- Readout Ancilla (RO) used to distinguise S-T transistion
- Transition detected by SET
- RO intialized and stored from and to the SET

Wiring

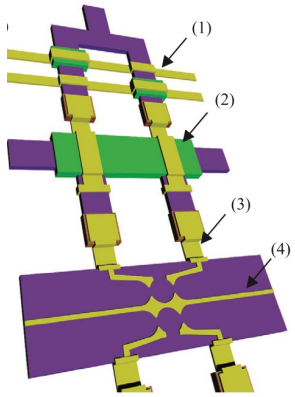
i) Sequential readout in a module
- All drains connected to a single line
- Plungers controled by global demux outside

ii) Simultaneous readout
- Amplitute modulation: Different bias Vp for each SET plunger
- Frequency mod: RF readout of SET -> Local resonators -> large size

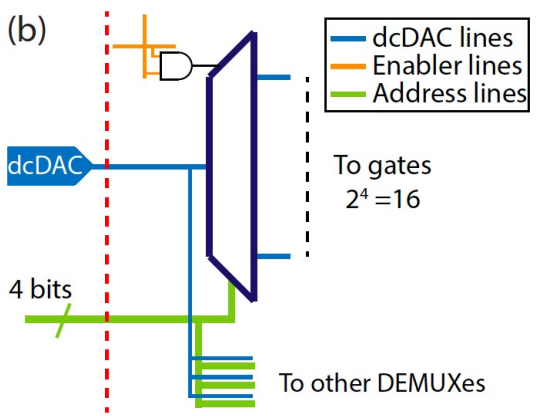
Local Control Electronics

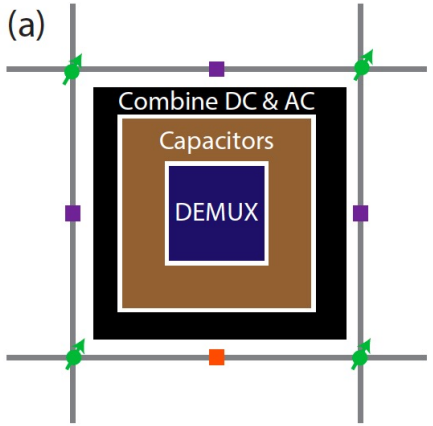


Y. Xu et al 2020



R.K. Puddy et al 2015



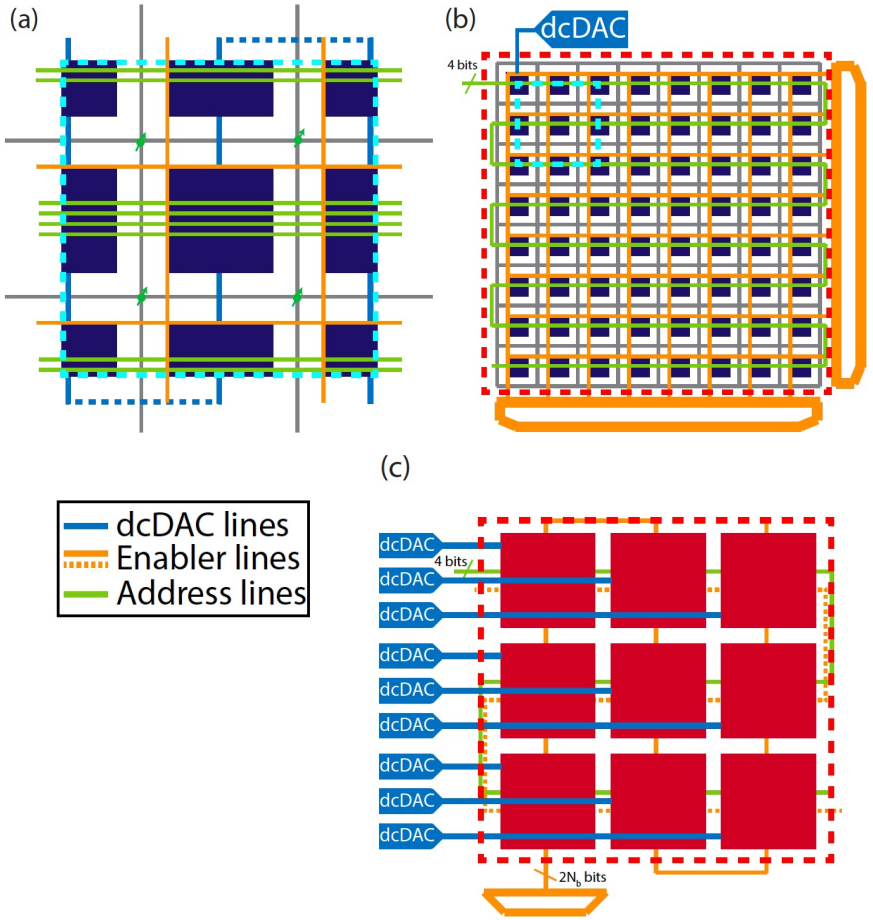


- Sample-and-hold scheme to apply a local DC bias to gates
- Two resolutions : Coarse (C) of ΔV=1uV (electron charge) & fine (F) ΔV=1mV (thermal noise)
- Two hold capacitors :C_c = 0.16 fF & C_F = 0.16 fF

- Enabler line for each demux and dcDAC connection

- 64 DC bias gates per unit cell
  - 1 to 16 demux (4 bits) in each open region
    - 4 demuxes per unit cell

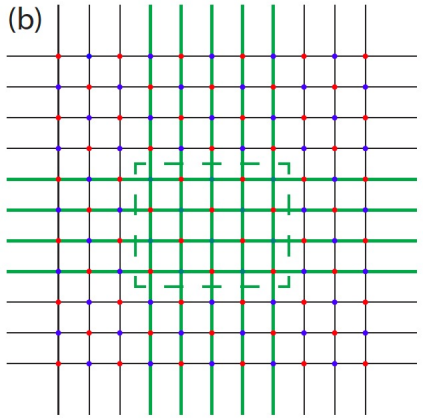
Local Control Electronics

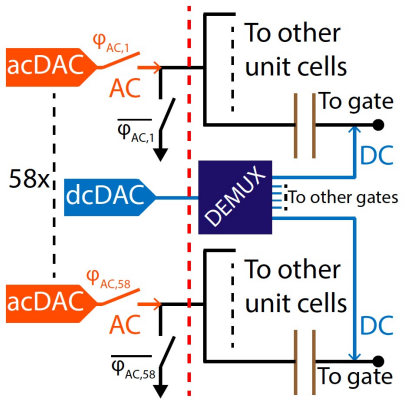


- Demux enabled by crossbar addressing – in-module sequentialy all modules in parallel
- All array updated in a single module refresh cycle

Gates	Routing
Shuttling (blue)	Source → gate
Pulsed (red)	DC: source → local demux & S/H → gate AC: source → gate
Sensing dot plunger (purple)	DC: source → local demux & S/H → gate AC: source → global demux → gate
Drain contacts	Measurement device ← Ohmic

Local Control Electronics





Type of line	unit cell	Connections at module	quantum plane
DC biasing	9	$4N_b + 5$	$M_b^2 + 4N_b + 4$
Shuttling	4	4	4
Pulsed signals & MW	58	58	58
Logical operations	$4x$	$4N_b x$	$4N_b M_b x$
Readout	3	$2\log_2 N_r - \log_2 r + 1$	$M_r^2 + 2\log_2 N_r - \log_2 r$
Total	$74 + 4x$	$4N_b(1+x) + 2\log_2 N_r - \log_2 r + 68$	$M_b^2 + M_r^2 + 4N_b(1 + M_b x) + 2\log_2 N_r - \log_2 r + 66$

- AC signals (MW and pulsed) generated remotely by acDAC before circuit that combines AC and DC
- Crossbar network design to control barrier gate to enable surface codes.

- 4 enablers + 4 address 1 dcDAC= 9 lines for biasing p.u.c.
- Only enabler scale with the # of u.c. as 4Nb per module
- Address lines and dcDAC shared between all u.c
- Shuttling (4) and AC signals (58) are shared in the array
- For crossbar depends on the encoding for logical qubits χ

Million Qubit Array example

Footprint

Capacitor A_C = 450 um^2
Demux (40 nm tech) = 180 um^2
Qubit pitch d = 12-14 um → 50nm QD pitch→ 260 QD per lattice arm

Heat Dissipation

- Parasitic capacitances of the routing lines $P_p = \frac{1}{2} C_p v_p^2 f_p$
- Discipation for the sample-and-hold circuits for 4 Demux p.u.c. $P_d < 140 \text{ nW}$
- AC thin lines power discipation $P_t = 1.1 \frac{\text{nW ns}^2}{\text{V}^2} (v_t f_t)^2$

Million Qubit Array:

- 2^{20} (10^6) qubits, or U = 2^{18} unit cells
- 256 modules maximum clock frequency of the demux biasing to f_b=6 GHz
- Rent's exponent = 0.43 + crossbar =0.5

Area covered by the quantum plane = 177 mm^2
Duration of a surface code cycle:

- Shuttling time t_{sh} 50 ns [B. Buonacorsi et al.]
- Gate time $t1_q$, t_{sw} =25 ns [R. C. C. Leon et al.]
- PSB Readout time t_r =1 µs [E. J. Connors et al.]

Total cycle time, t_{sc} =6 µs < T_2^* =20 µs

Power discipation 100mW → 0.2 K self heating

Thanks!!