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Gating a Quantum Dot through the Sequential Removal of Single Electrons from a Nanoscale Floating Gate

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We use the tip of an atomic force microscope (AFM) to charge floating metallic gates defined on the surface of a Si/SiGe heterostructure. The AFM tip serves as an ideal and movable cryogenic switch, allowing us to bias a floating gate to a specific voltage and then lock the charge on the gate by withdrawing the tip. Biasing with an AFM tip allows us to reduce the size of a quantum dot floating-gate electrode down to approximately 100 nm. Measurements of the conductance through a quantum dot formed beneath the floating gate indicate that its charge changes in discrete steps. From the statistics of the single-electron leakage events, we determine the floating-gate leakage resistance $R \sim 10^{19}$ Ohm—a value that is immeasurable by conventional means.

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Device

Motivation

- Problem: growing # RT control lines

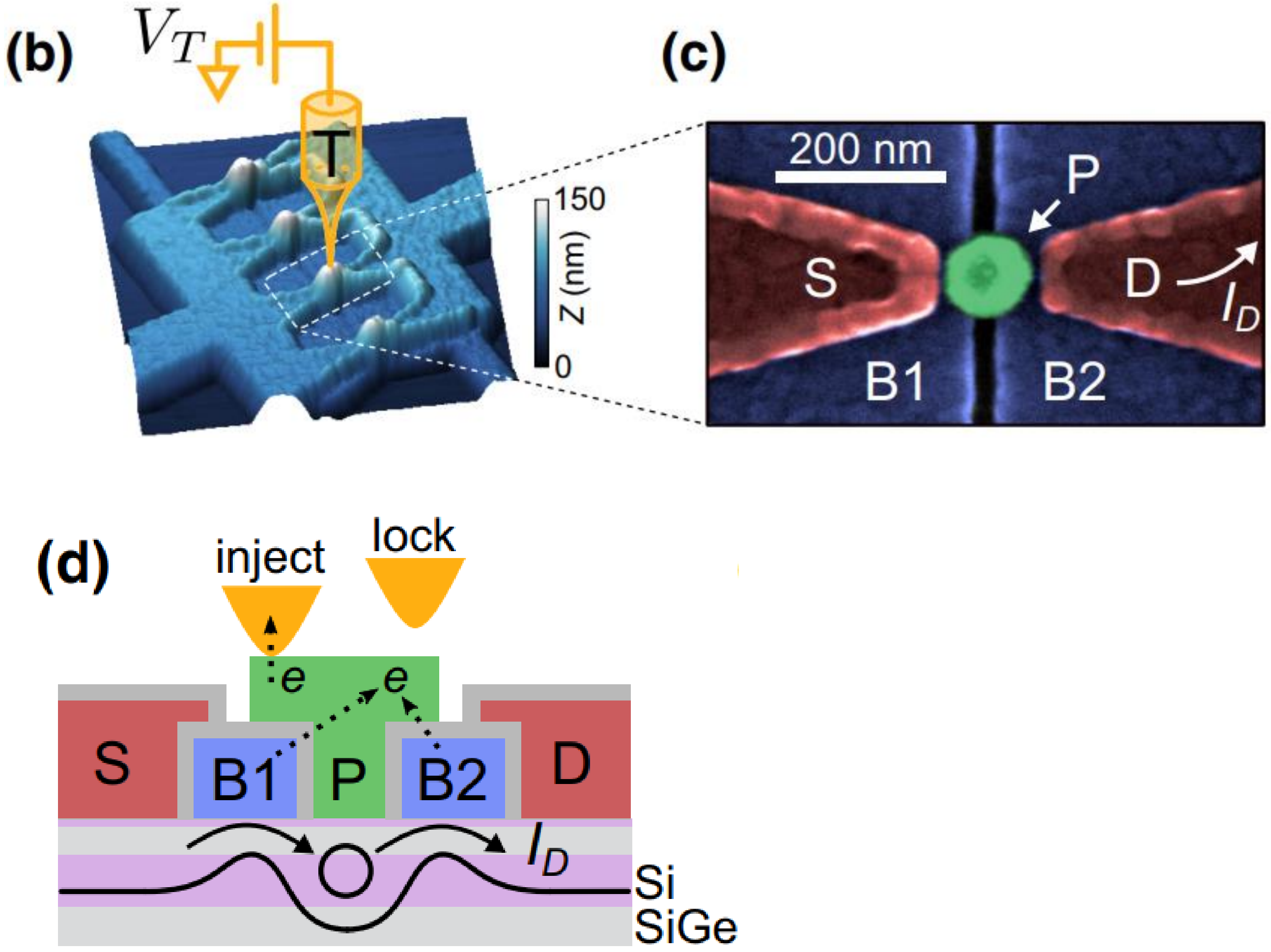
- Solution: Sample-and-hold circuit (Charge floating gate)
    - Zero resistance switch
    - High electrical insulation
    - To date achieved only using FETs in:
      GaAs, Si/SiGe, CMOS QDs

Device:

- Accumulation-mode (undoped Si/SiGe heterostructure)
  2nm Si Cap
  50nm $Si_{0.7}Ge_{0.3}$
  5nm Si quantum well

- 3 Gate Layers:

Al barriers	B1,B2
Al accumulation	S,D
Pd plunger	P (good AFM tip contact)



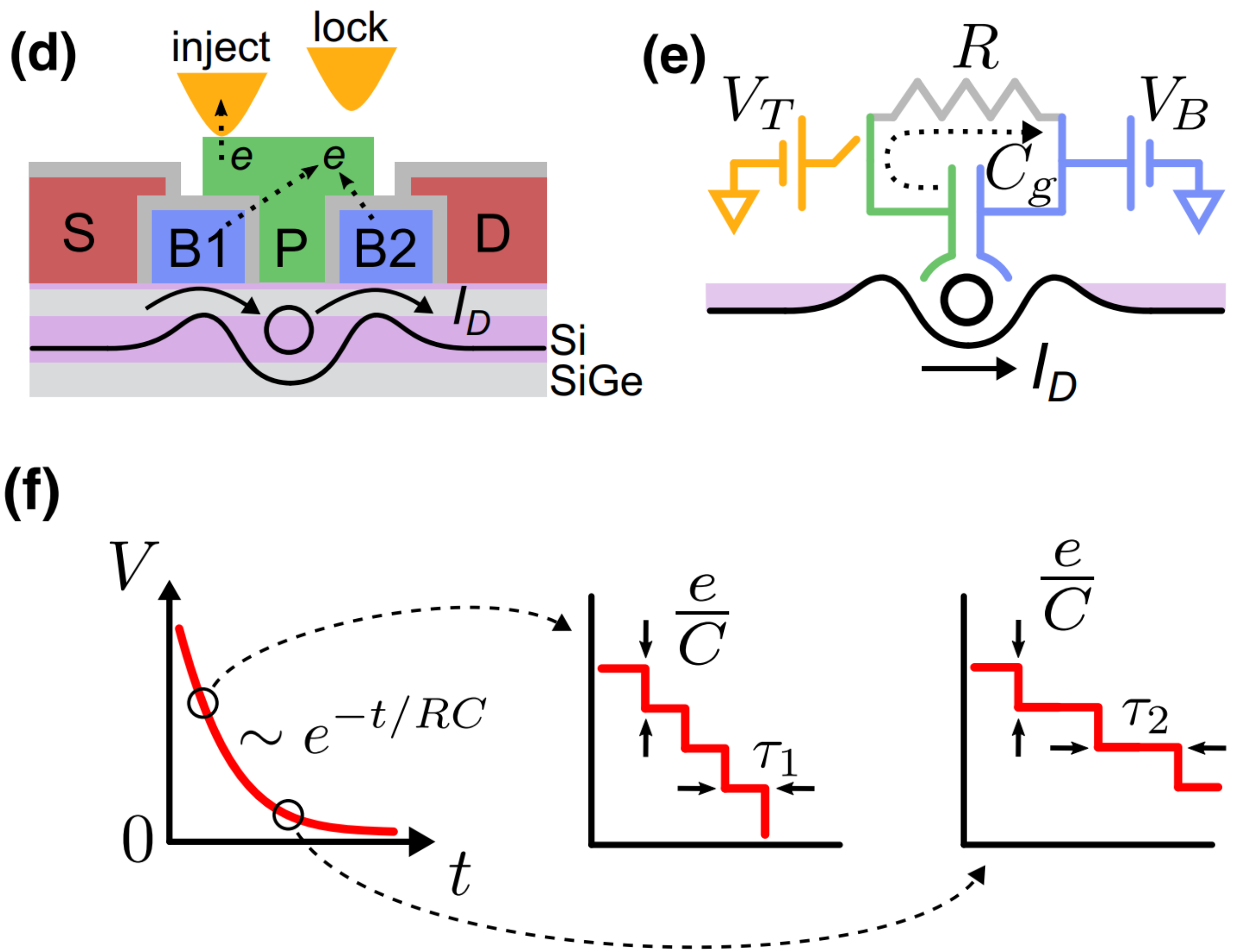
Discharge floating gate

Floating gate discharge

Floating gate: Charged capacitor

Classical discharge: $V \sim e^{-t/RC}$
=> combined RC time

QM limit: discrete Steps (single e-tunnelling)
$\Delta V = e/C$
$\langle \Delta t \rangle = \tau$



Operation continuous vs lock

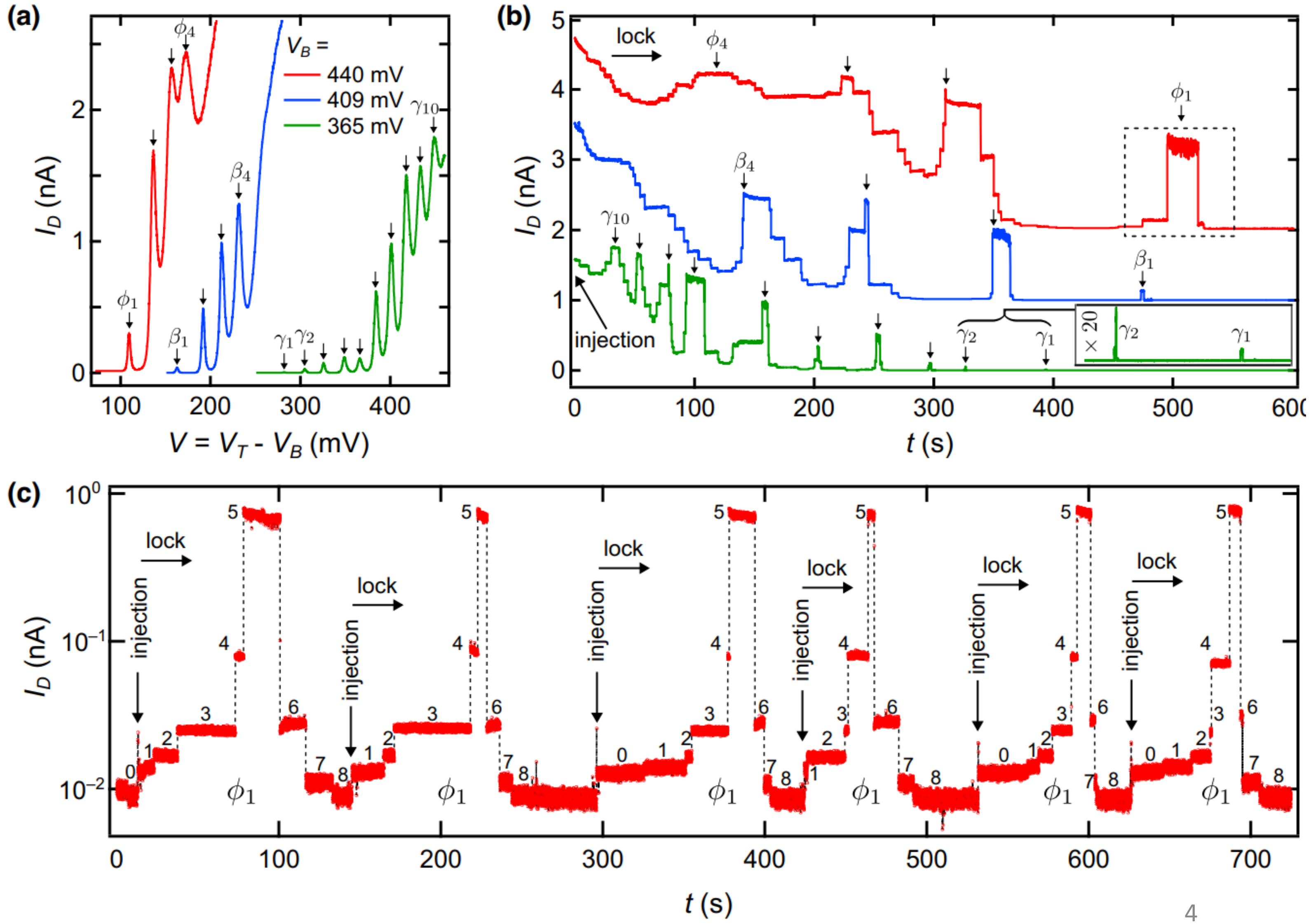
Contact mode:
Bias gate with AFM tip (regular gate)

Charge lock:
Retract biased tip (200nm)
Gate discharges over time
=> retraces CB peaks

Gate small => discrete discharging steps
1e tunnelling to B1(B2)

=> gate resolution limited to ~1mV
(few e QD: remove few 100e from gate)

Reproducibility (ϕ1)
Same # discharging steps
(2 missing out of 50)
=> mostly single e⁻ tunnelling



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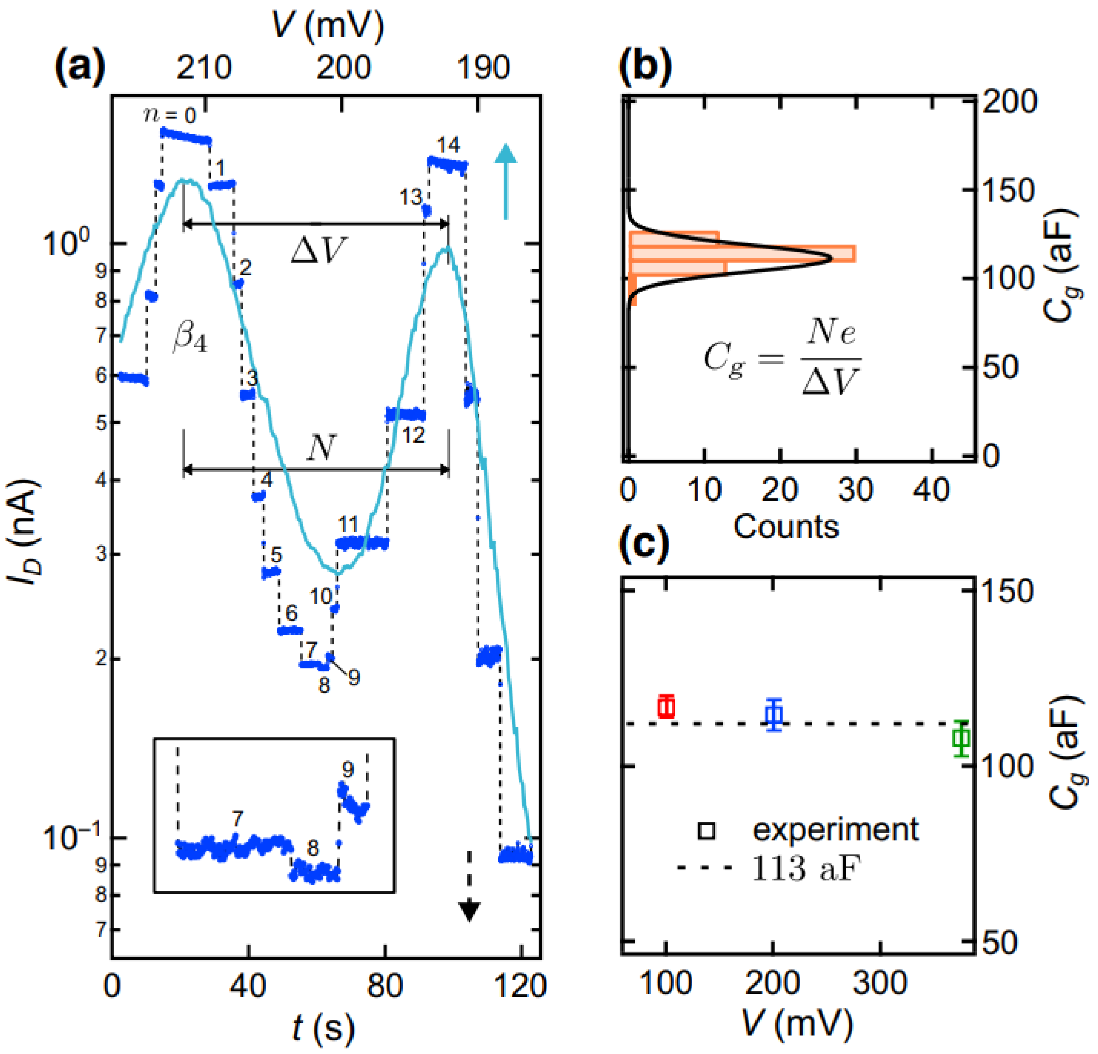
Operation continuous vs lock

Contact mode vs charge lock:
Bias gate with AFM tip (regular gate)

Smaller CB amplitude than charge lock
enhanced T_e due to AFM contact?

Capacitance of gate:

- $C_g = Ne/\Delta V$ (~14 electrons needed btw peaks)
  => C_g ~ 112 aF
  (C_{gQD} ~ 10 aF; 1 electron btw peaks added)
- C indep. V (gate geometry)
  Slight drop: change of QD size
- 16'000 times larger capacitance precision than previous e-counting methods
- 1000 smaller footprint floating gates compared to FET
- $\Delta t = R*C_{stray}$ (takes 1000 longer to measure same R wit FET)



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Fano factor

Fano factor definition:

For a counting process after time t the Fano factor is:

$$F(t) = \frac{\sigma_t^2}{\mu_t}$$

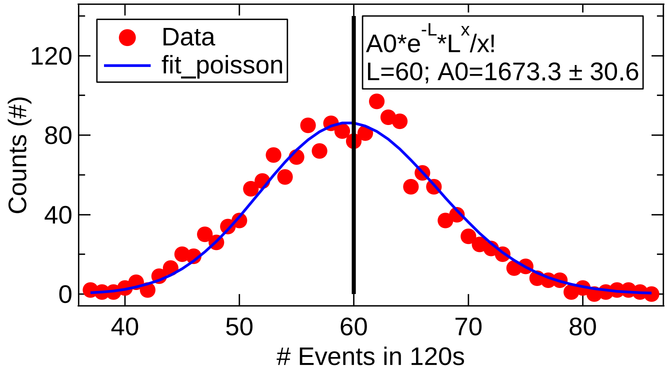
t :	time
σ_t^2:	variance
μ_t :	mean

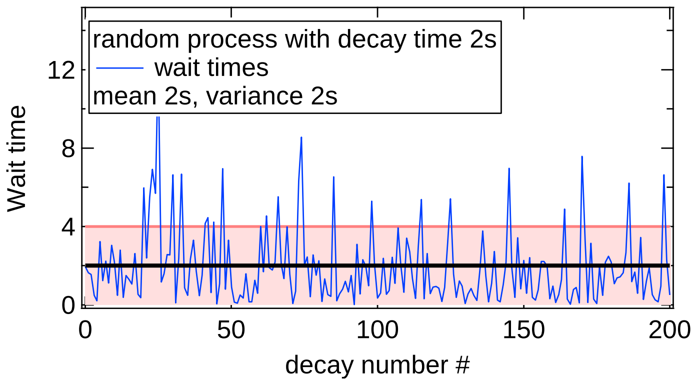
$$P(t) = \frac{e^{-\frac{t}{\tau}}}{\tau} \Rightarrow \int_0^\infty P(t)dt = 1$$

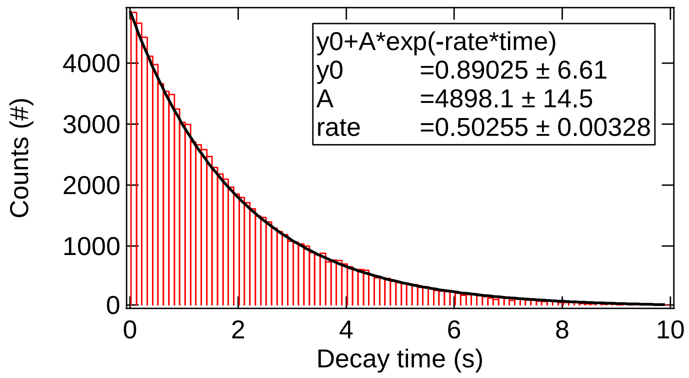
$$E = \int_0^\infty t \cdot P(t)dt = \tau$$

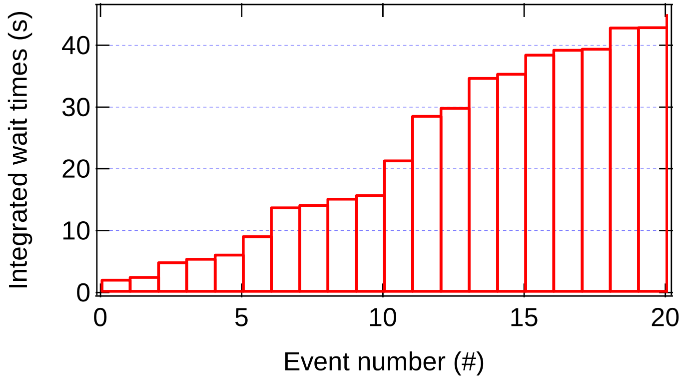
$$Var = \sqrt{\int_0^\infty (t-\tau)^2 \cdot P(t)dt} = \tau$$

- Likelihood of an event occurring in any time interval is equal for all time:
  => Holding times exponentially distributed (sigma = mean)
  => Poisson counting process (F=1; F=0 for constant function)





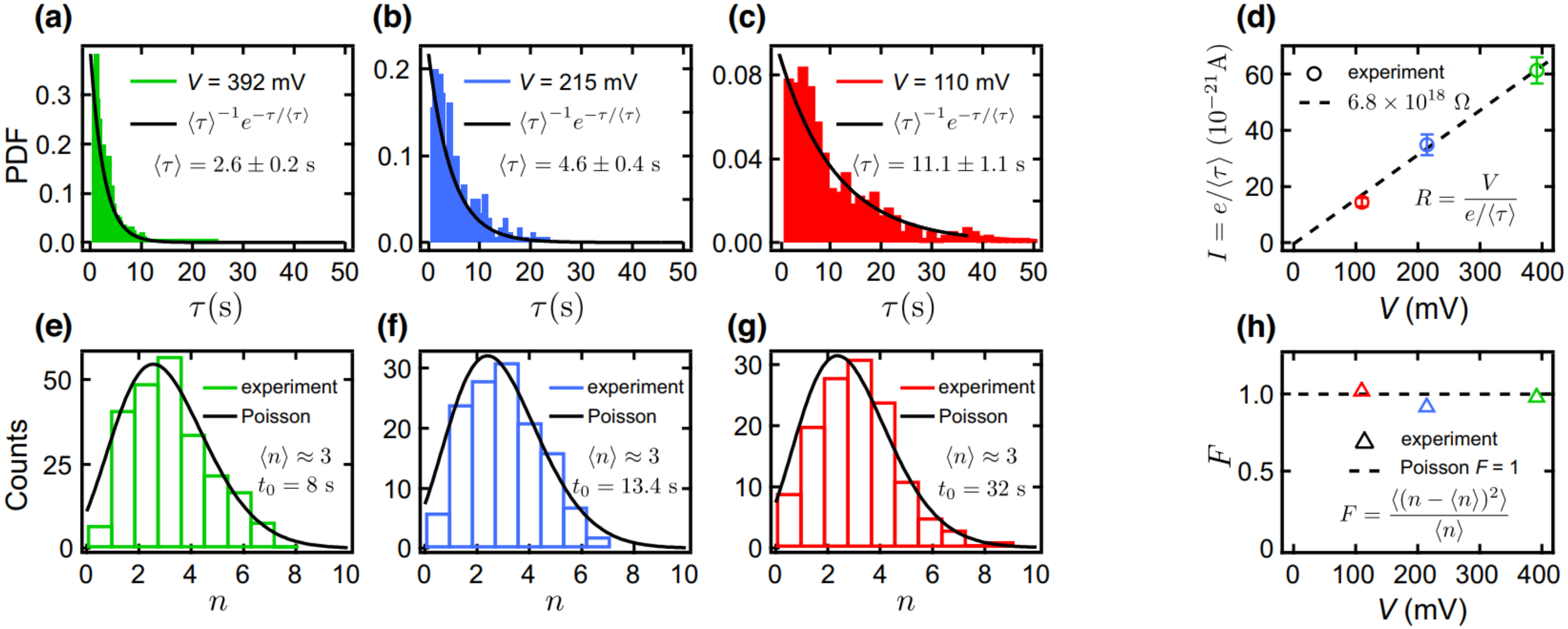




Tunnelling statistics

Uncorrelated electron tunneling

- Uncorrelated tunnelling: exponential waiting time distribution
  I = V/R = e/<τ> => <τ> ~ ΔV
- Second moment expected to be poisson-distr. (Fano factor 1)



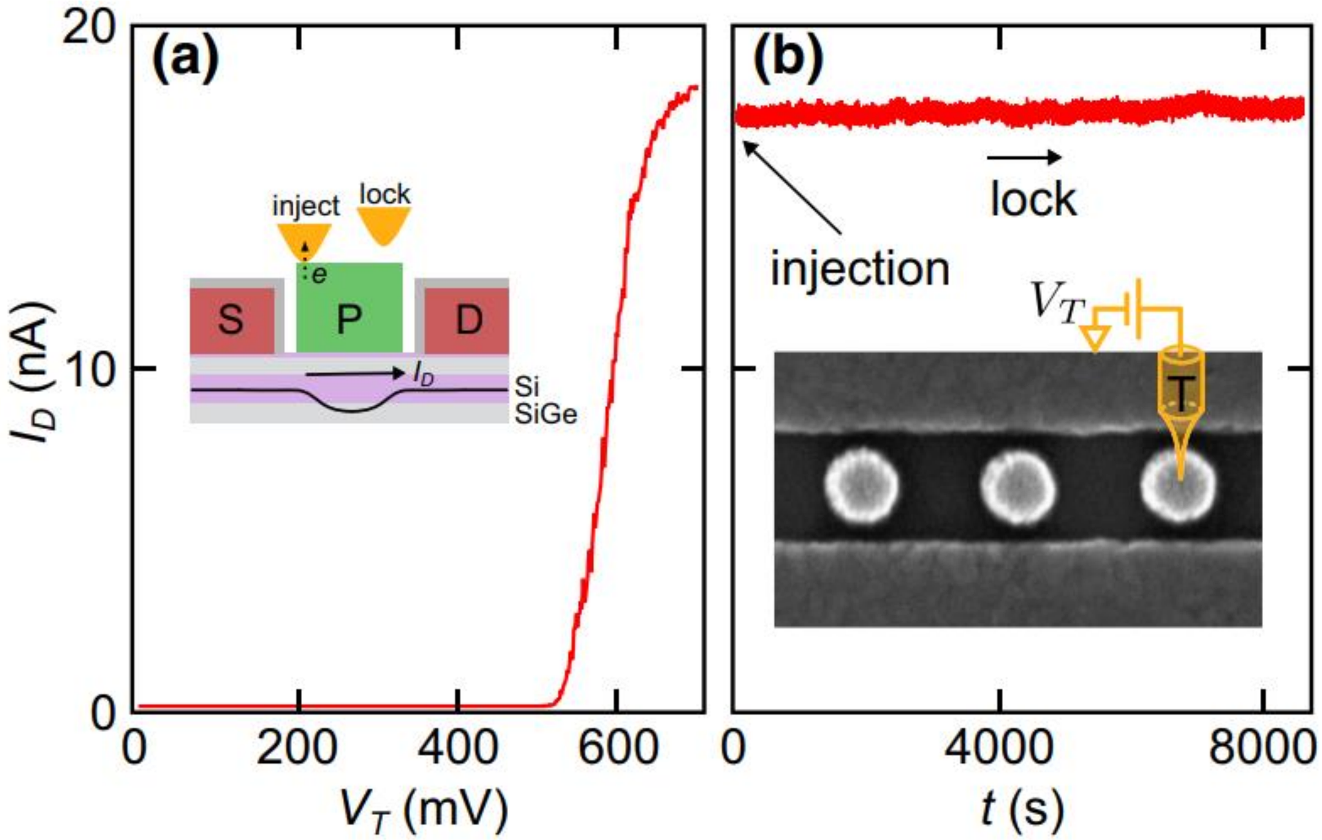
Single layer device

Device

- Single gate layer (S,D,P)
- No barriers
- Transistor like turn-on curve
- Floating gates sit directly on Si substrate
  Substrate: only leakage path

- Charge retention:
  Tens of e- leaking during hours

- Future: thicker oxide



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Summary

- Gate locking demonstrated using AFM + floating gate
- Few 100s hold-time in QD device (interleaved gates)
- Hours hold-time in 1L device (transistor) without noticeable decay
- AFM allows for extremely small foot-print (100nm disc): 113aF, 200 electons to accumulated dot
- Very large leakage resistance to barrier determined by counting statistics (6,8e18 Ohm)
- Counting statistics: Poisson process, Fano factor = 1