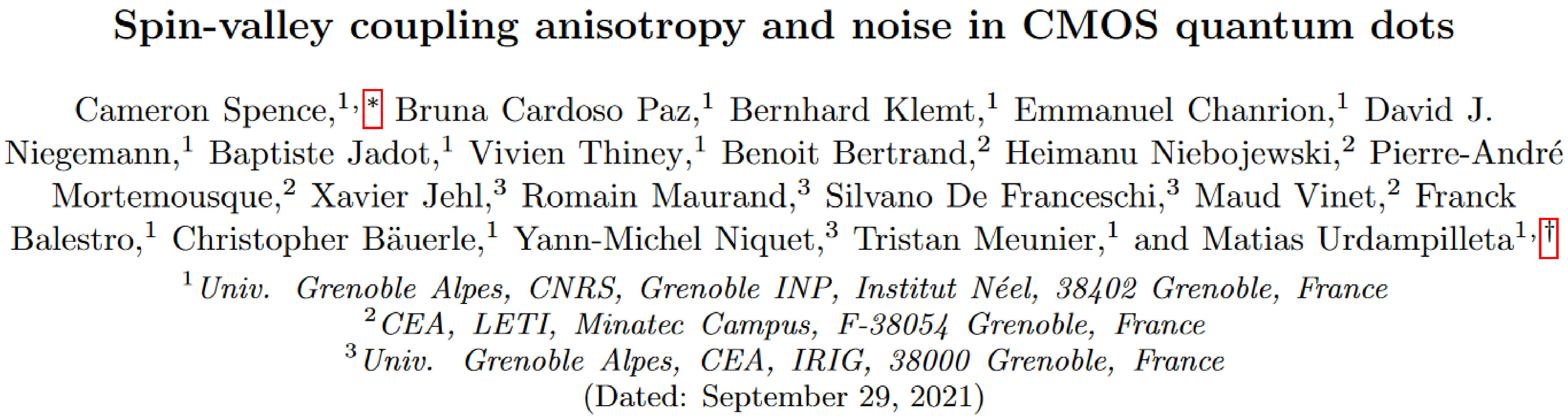

Spin-valley coupling anisotropy and noise in CMOS quantum dots

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Outline

- Spin characterization in CMOS nanowire devices
- Determination of valley splitting via T_1 measurement
- Anisotropy of spin-valley mixing
- Investigation of charge noise (on valley-splitting)

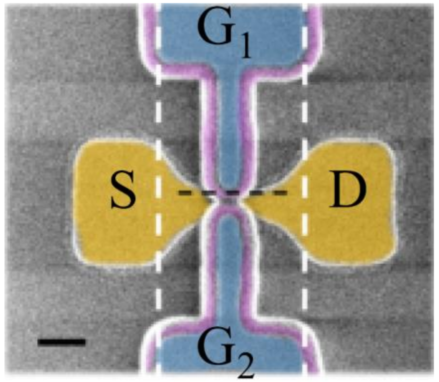
Device

- Electrons in CMOS nanowire (width 90 nm, thickness 15 nm), fabricated on 300mm foundry-compatible wafer

- Pair of split front gates (50 nm length, separated by 50 nm)

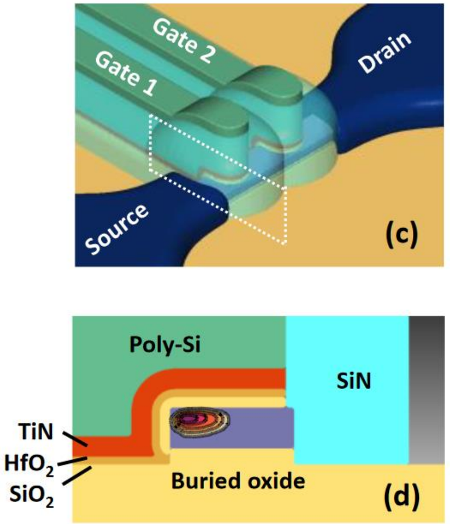
- Electron reservoirs formed by…
    - Device 1: Ion implantation
    - Device 2: In situ growth of degenerate n-doped Si

- 6 nm $\mathrm{SiO_2}$, 5 nm TiN between channel and gates



- Metallic top gate (white dashed line) 400 nm above channel, biased to +2V
- Polarized silicon bulk below buried oxide used as back gate at +5V

Sketch of similar type of device:

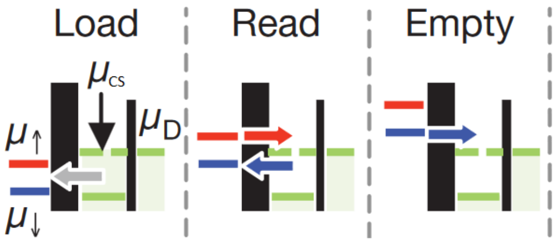


From [1]

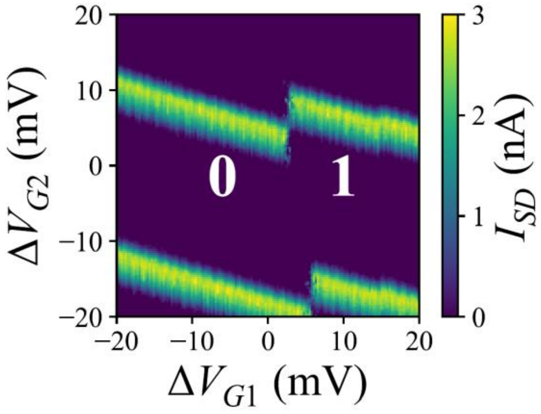
[1] L. Bourdet et al., IEEE Trans. Electron Devices (2018)

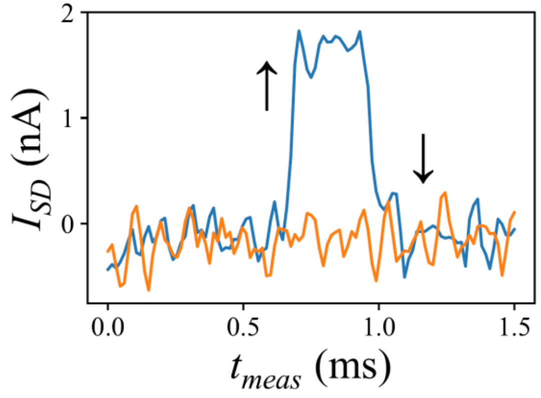
Readout of spin state

- Energy-selective readout scheme



From [2]





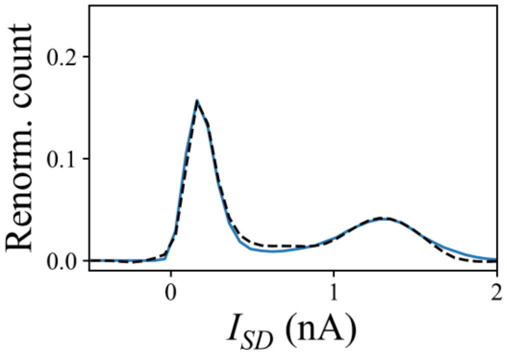
- Binned histogram of maximum I_{SD}

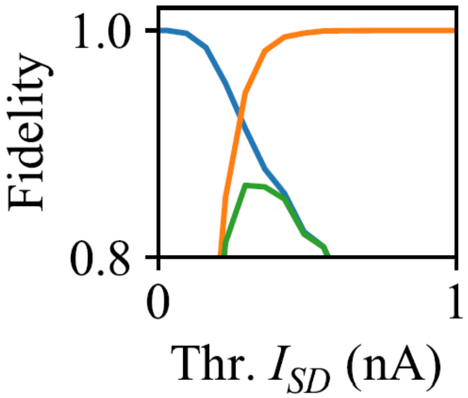
To determine ideal threshold current I_{thr} , calculation as in Ref. [2]:

$$F_\downarrow = 1 - \int_{I_T}^{\infty} N_\downarrow(I)\mathrm{d}I$$

$$F_\uparrow = 1 - \int_{-\infty}^{I_T} N_\uparrow(I)\mathrm{d}I$$

$$V = F_\downarrow + F_\uparrow - 1$$





Avg. readout fidelity above 92%, and 86% visibility

[2] A. Morello et al., Nature (2010)

T_1 measurements & valley splitting

- Load electron with random spin orientation, then probe spin up population after given waiting time

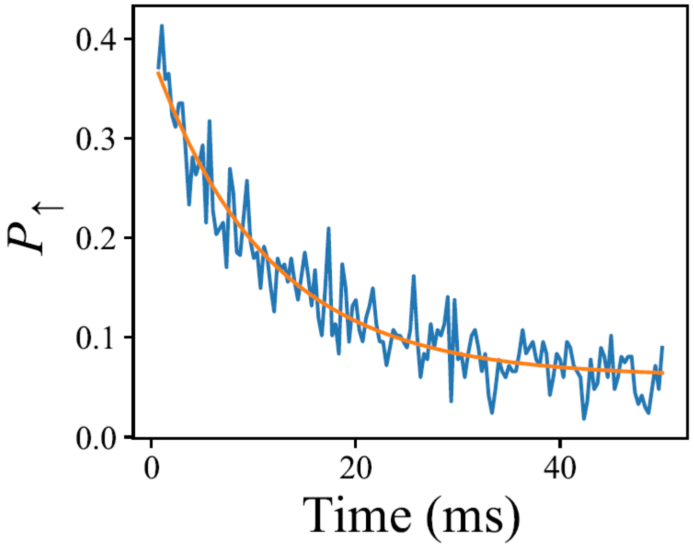
- Hotspot in relaxation rate where E_{VS} matches E_Z

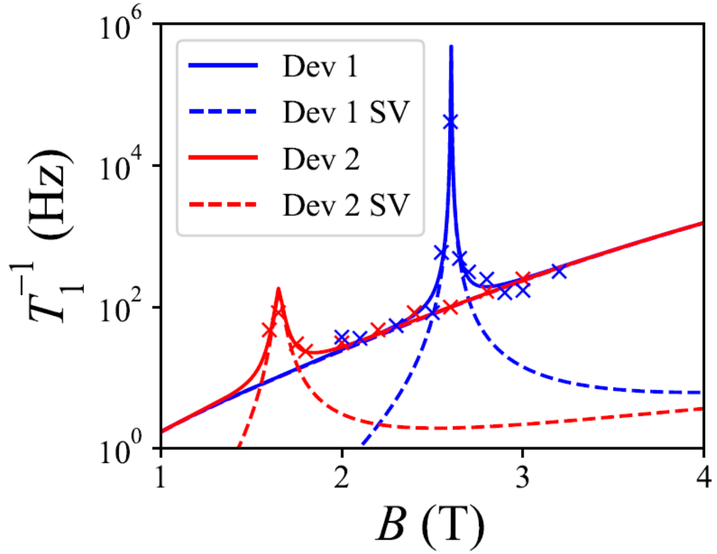
- Fit to model from Ref. [3]:

$$T_1^{-1} = \Gamma_{Ph,SV} + \Gamma_{JN,SO} + \Gamma_{Ph,SO}$$

$\Gamma_{Ph,SV}$: Relaxation rate due to spin-valley mixing & coupling to phonons
$\Gamma_{JN,SO}$: Relaxation rate due to SO-coupling via Johnson-Nyquist (thermal) noise
$\Gamma_{Ph,SO}$: Relaxation rate due to SO-coupling via phonons

- Phonon-mediated mechanism dominates at high fields ($\Gamma_{JN,SV}$ neglected)





→ $E_{VS} = 300 \pm 13$ μeV

→ $E_{VS} = 191 \pm 16$ μeV

→ SV-anticrossing gap of
0.2 ± 3 μeV (4.0 ± 3 μeV) (?)

Similar rates outside hotspots indicate similar overall structure of quantum dots in the 2 devices

[3] P. Huang et al., PRB (2014)

Anisotropy of spin-valley mixing

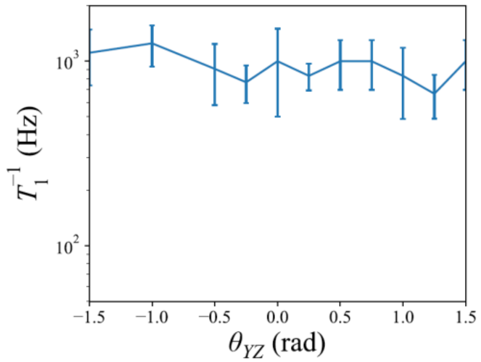
- SV-mixing expected to vanish in presence of >1 mirror planes

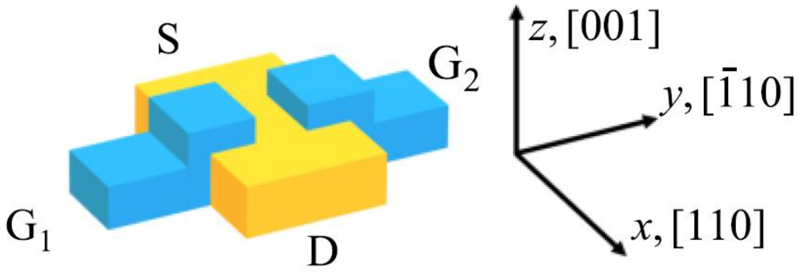
- Presence of hotspot indicates lower symmetry

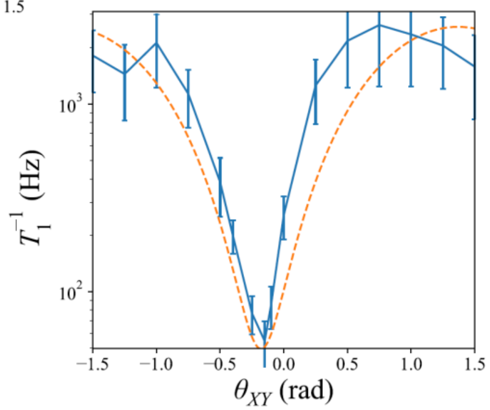
- It is expected that spin-valley mixing vanishes for **B**‖**x**, and remaining projection leads to

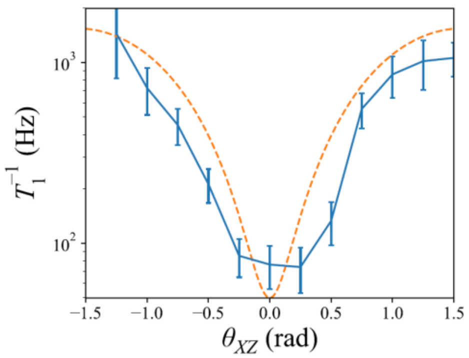
$$|\langle v_1 \uparrow| H_{\mathrm{SOC}} |v_2 \downarrow\rangle|^2 \propto \sin^2\theta$$

- **XY**-plane: NW axis not perfectly aligned with coil axes
- **XZ**-plane: different due to 2nd order anisotropy of gate overlap









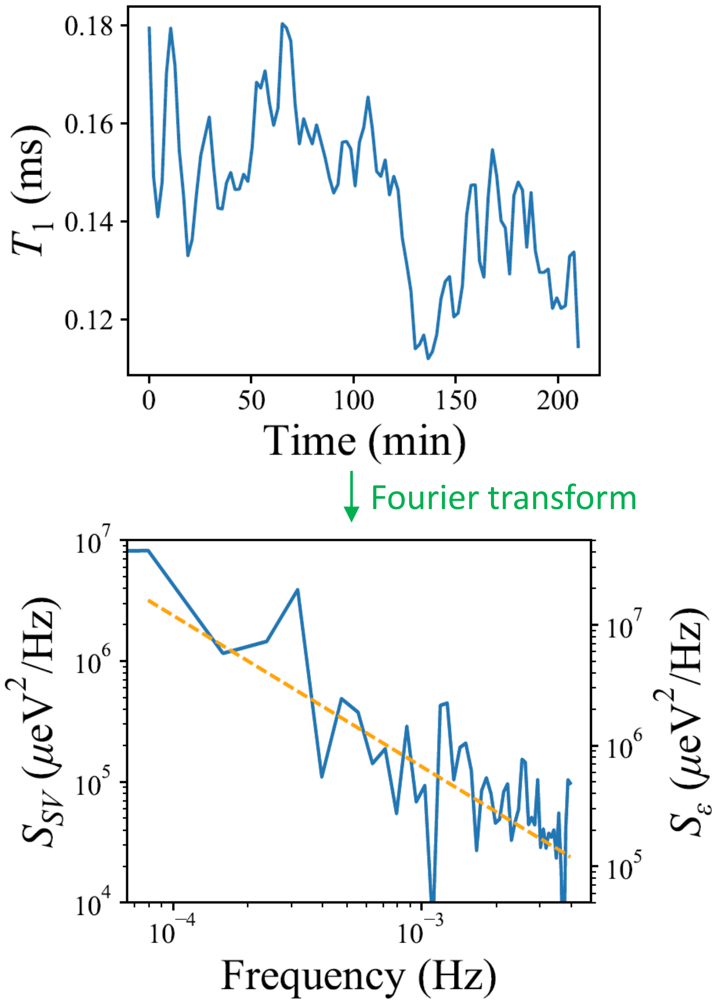
(at B-field close to hotspot)

Effect of charge noise on spin-valley mixing

- Valley splitting arises from strong confinement against top interface -> sensitive to electric fields; assume linear dependence for small noise amplitude

- Sit next to hotspot and record time evolution of T_1

- PSD follows 1/f dependence: $23\mu\mathrm{eV}^2/\mathrm{Hz}$ extrapolated at 1 Hz, corresponding to fluctuation of spin precession ~$0.6\ GHz/\sqrt{Hz}$
  - ➢ faster than hyperfine decoherence rate in nat. Si
  - ➢ On the order of dec. rate in charge and valley qubits



Summary

- Fast & reproducible spin characterization in CMOS nanowire devices
- Similar SOI-induced relaxation rates in both devices (outside of hotspots)
- Anisotropy measurement of spin-valley coupling via relaxation, strong symmetry plane ⊥ NW axis
- Strong low-frequency fluctuations could be detrimental for operation as spin-valley or valley qubit