A four-qubit germanium quantum processor

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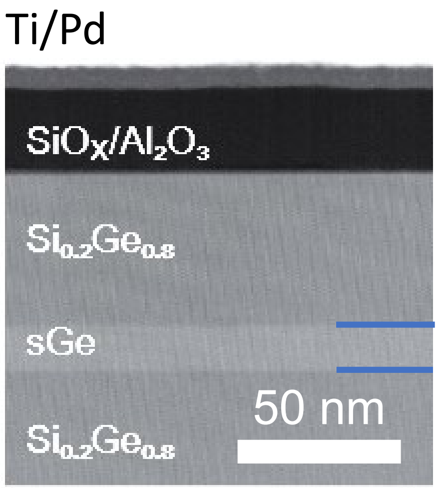
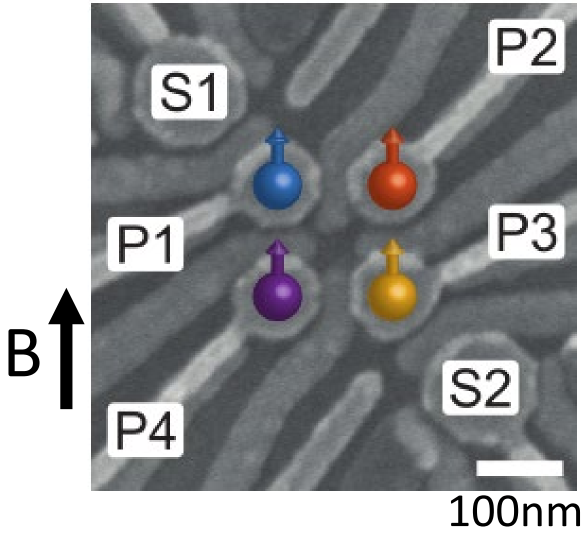
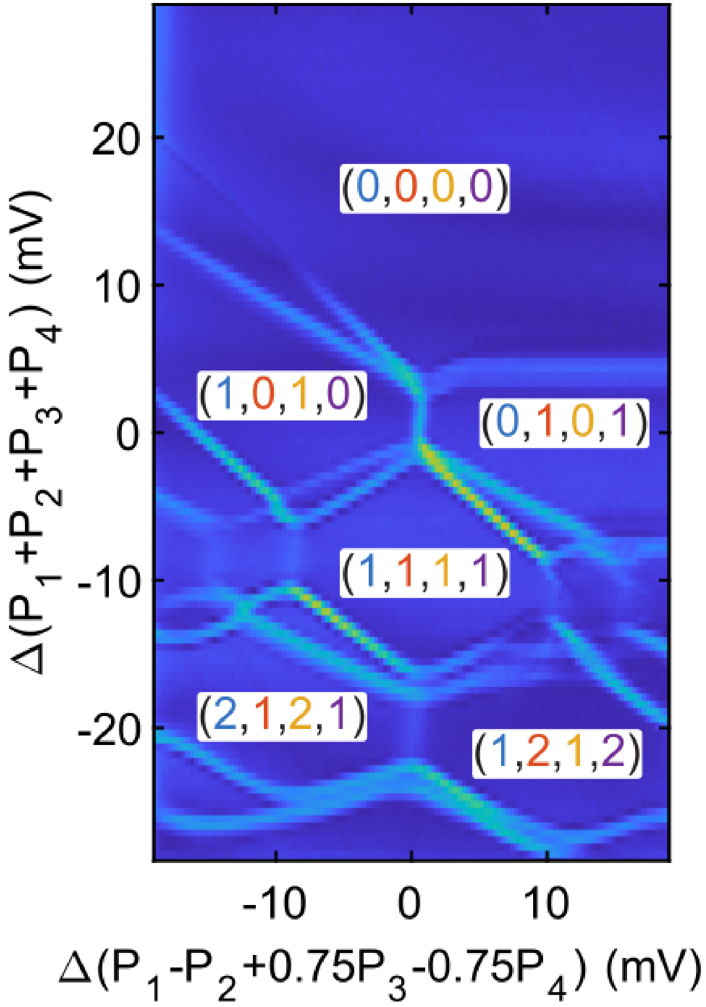
The device

- **heterostructure**: 55nm deep, 16nm thick sGe well
- two layers of Ti/Pd top gates, separated by 7nm Al_2O_3
- accumulate **6 hole QDs** (4 single hole QDs + 2 sensor QDs)
- set of virtual gates and barriers for independent tuning of occupancy and tunnel rates
- T_{base} = 20mK
- B ~ 1T is parallel to B_{SO}





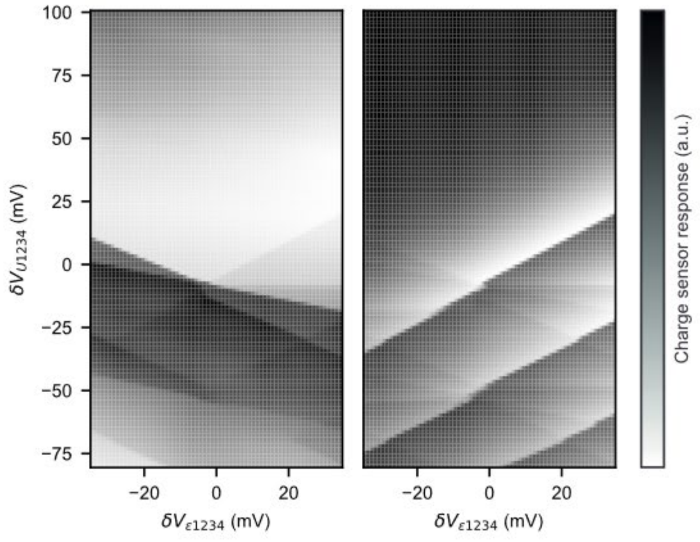


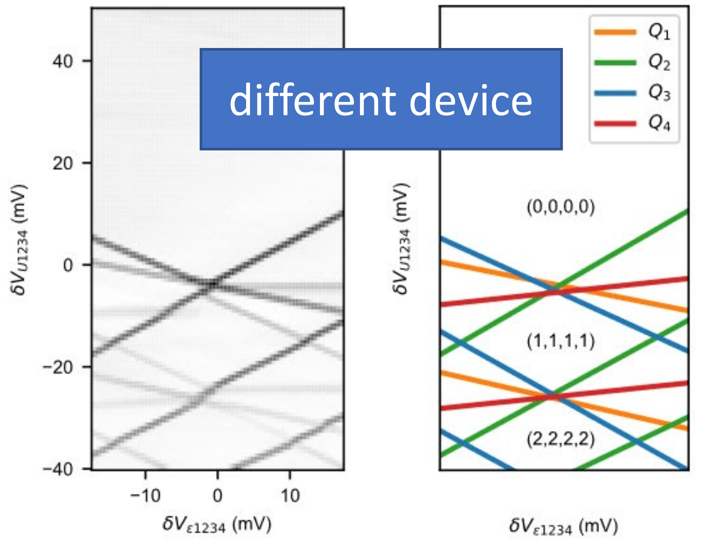
[1]Lodari, Hendrickx *et al*, arXiv:2007.06328

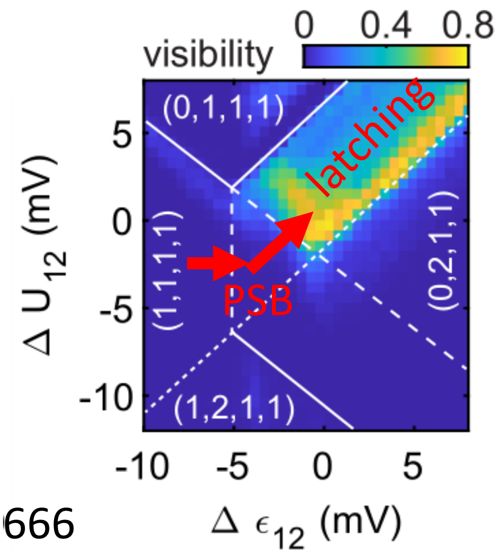
RF charge sensors

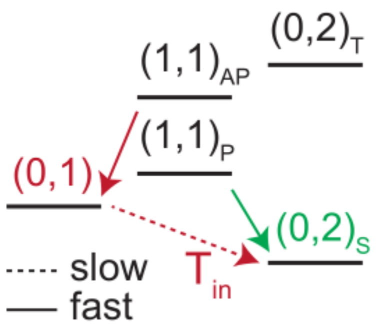
- two RF **charge sensor** QDs coupled to external tank circuits (NbTiN inductors)
- combine signal of both sensors for 4 dot charge readout

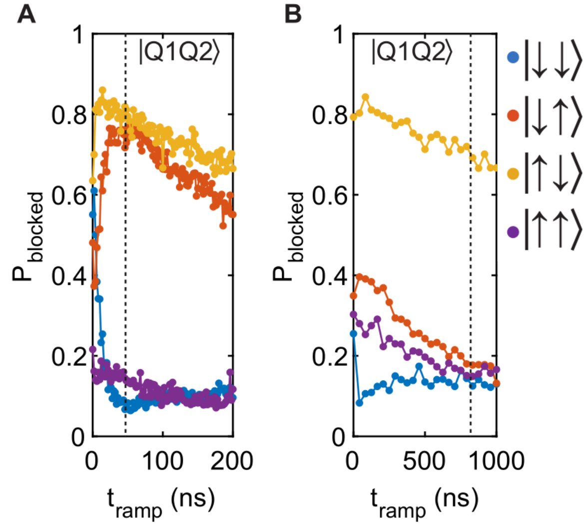
- **spin readout** via PSB + latching
- two readout modes:
  - parity readout **A** (parallel spins |↑↑⟩ |↓↓⟩ are blocked)
  - single state readout **B** (only |↑↓⟩ not blocked)







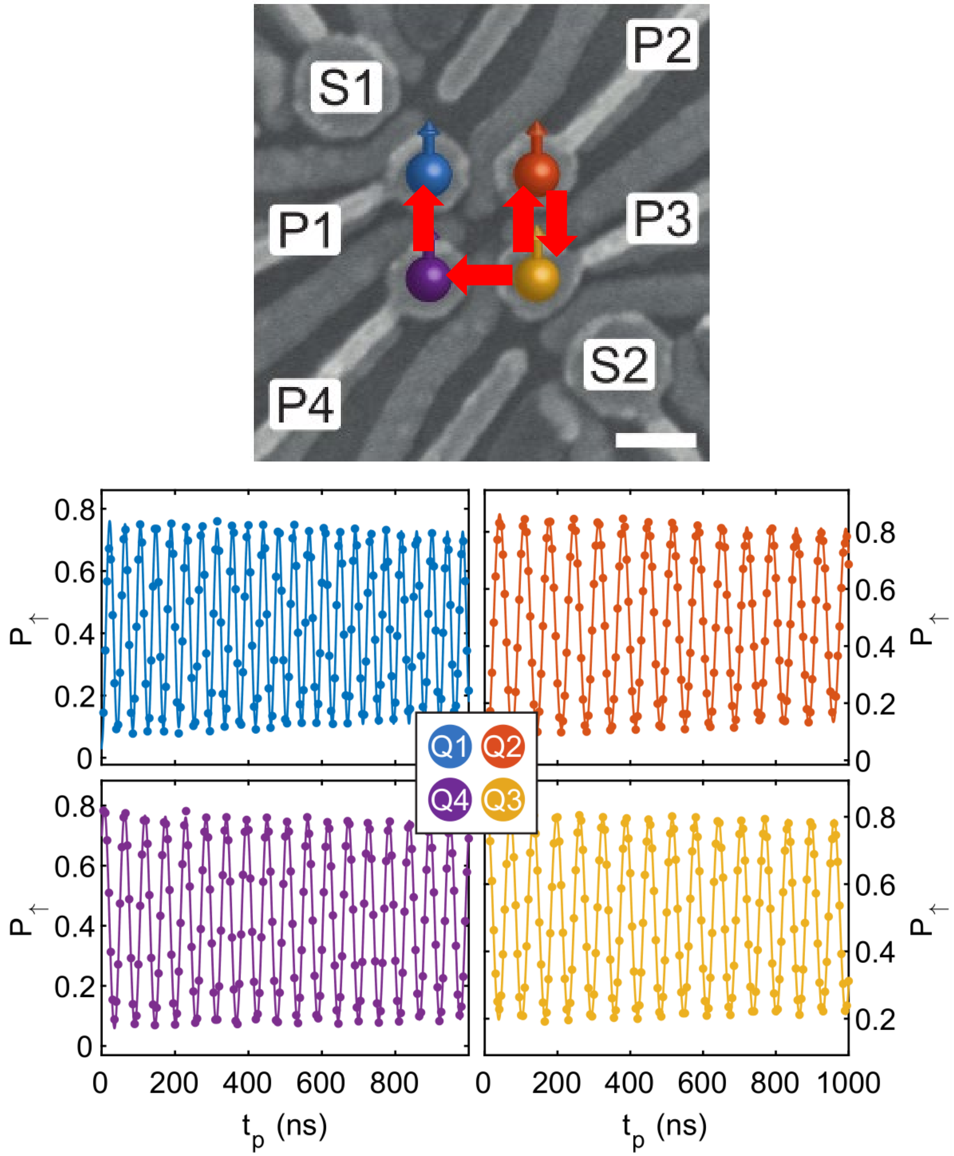




[2]van Riggelen, Hendrickx et al, arXiv:2008.11666

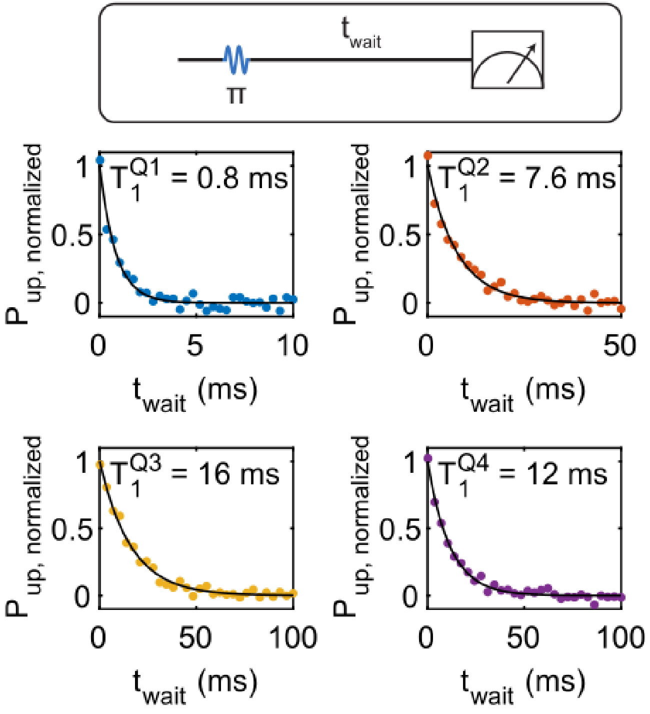
Four qubits

- encode qubit in **single hole spin**
- spin-orbit mediated EDSR
- EDSR with V(t) on neighbouring gates
- initialise in |↓↓↓↓⟩
- g-factors ~ 0.16 to 0.26
- Rabi frequency ~ 20MHz

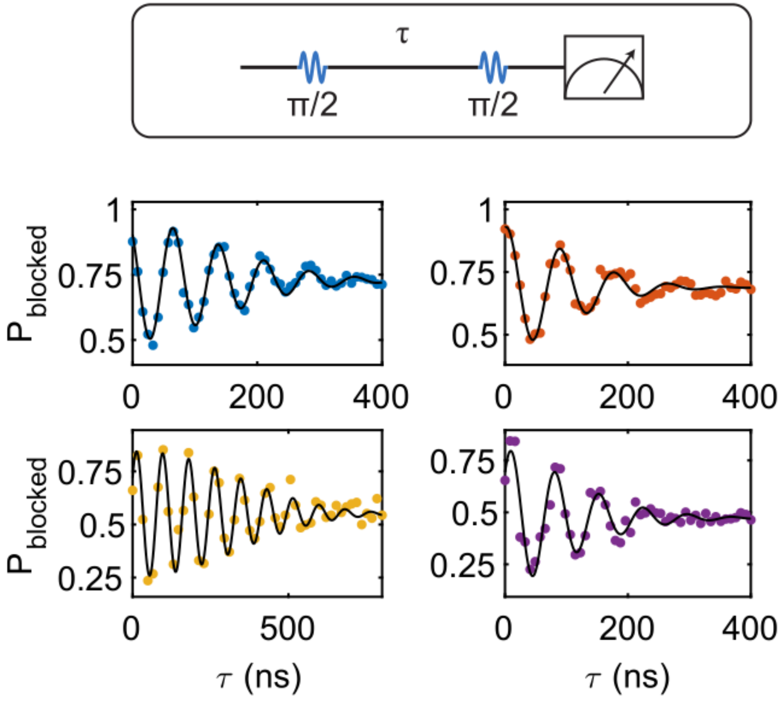


Single-qubit characterisation

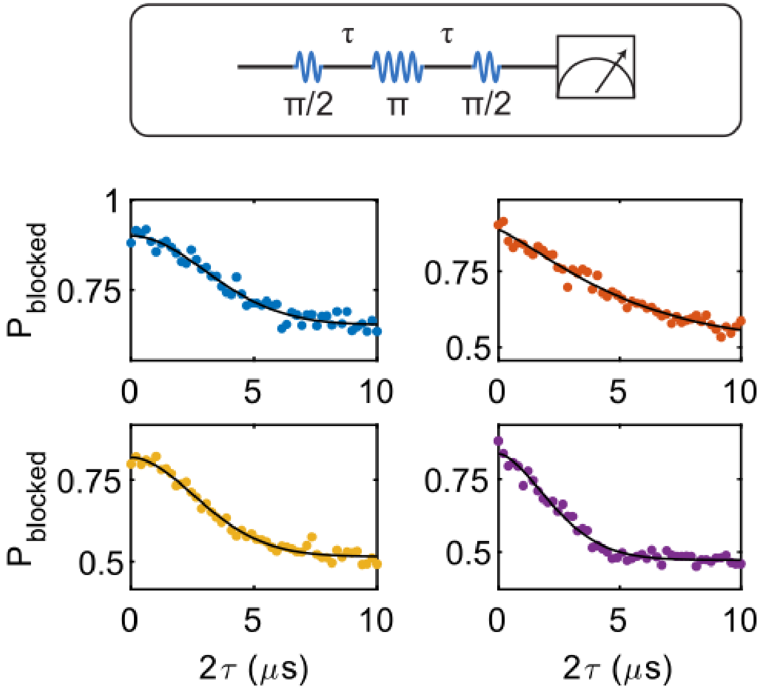
T_1 ~ 10ms



T_2* ~ 230ns



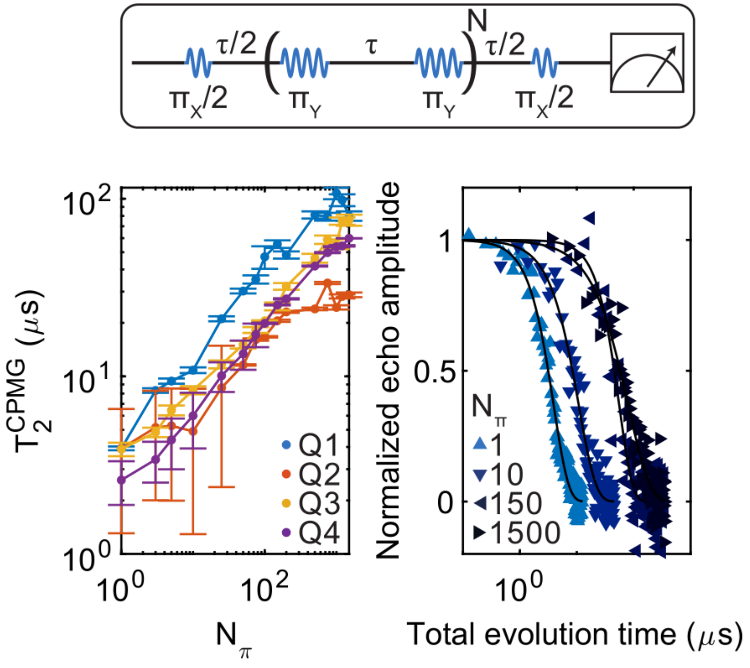
T_2^{Hahn} ~ 4µs



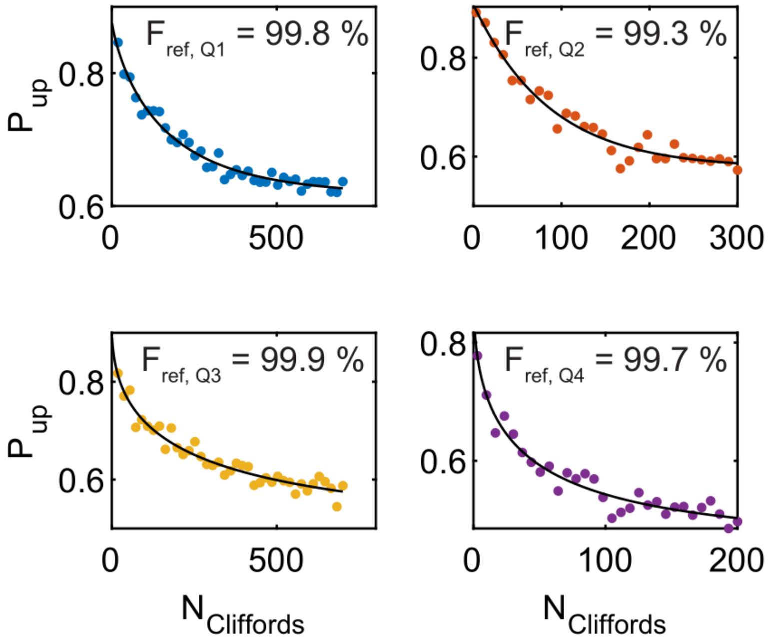
Rabi frequency ~ 20MHz

Single-qubit characterisation

T_2^{CPMG} ~ 100μs

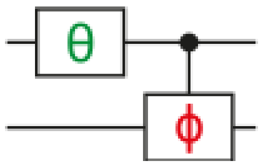


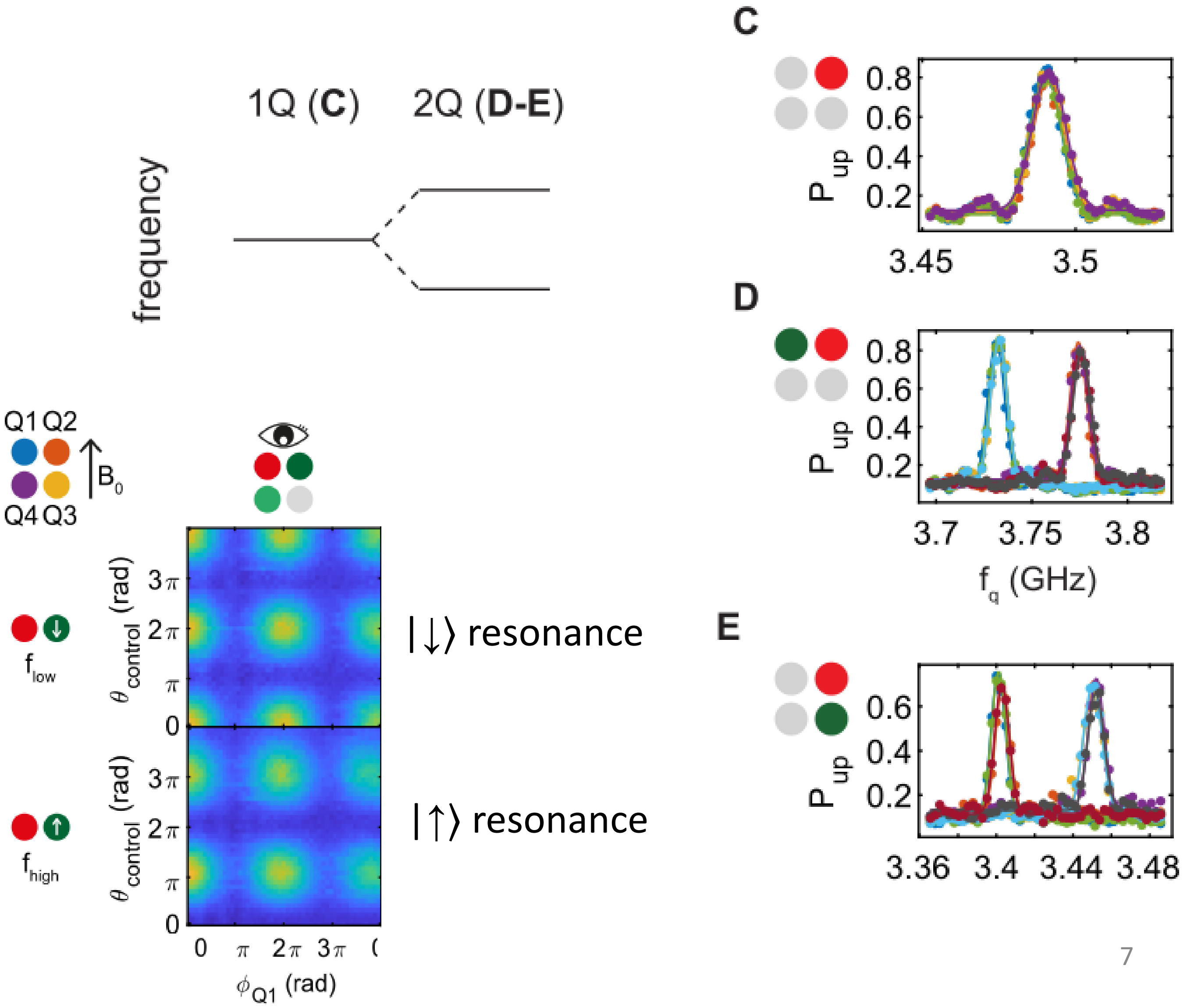
single-qubit single gate fidelity ~ 99.7%

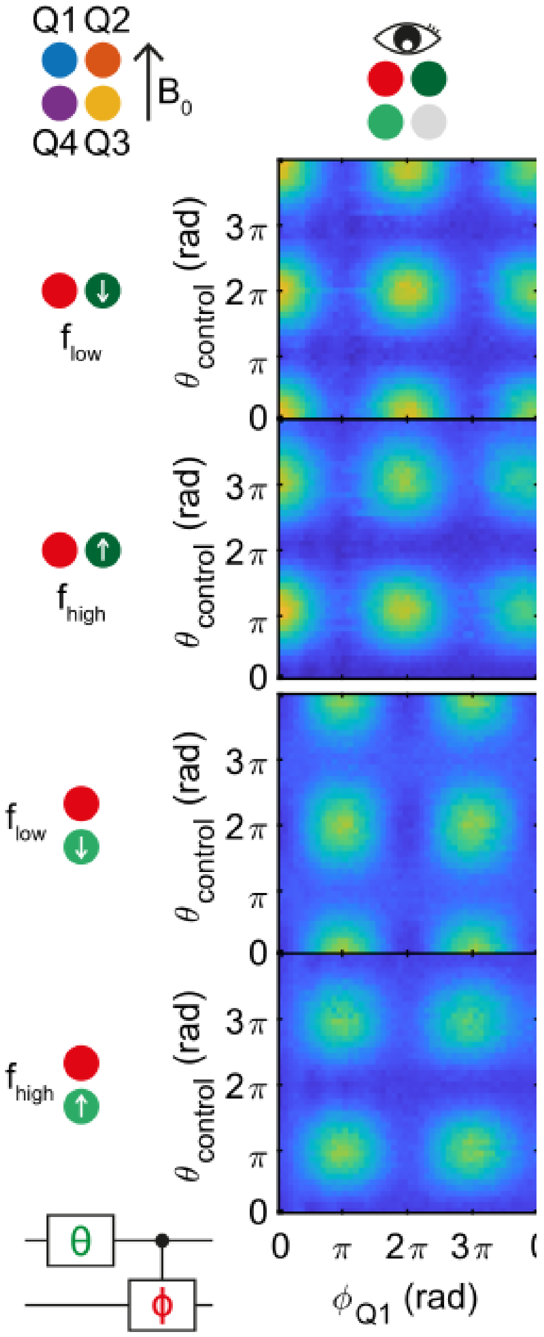


2-qubit gates: CROT

- universal QC possible with single and 2-qubit gates, e.g. CROT
- use virtual barrier to enable **exchange interaction** between neighbouring qubits to split resonance frequency
- **CROT** = rotate around x if control qubit is e.g. $|\downarrow\rangle$
- CX gate in 100ns

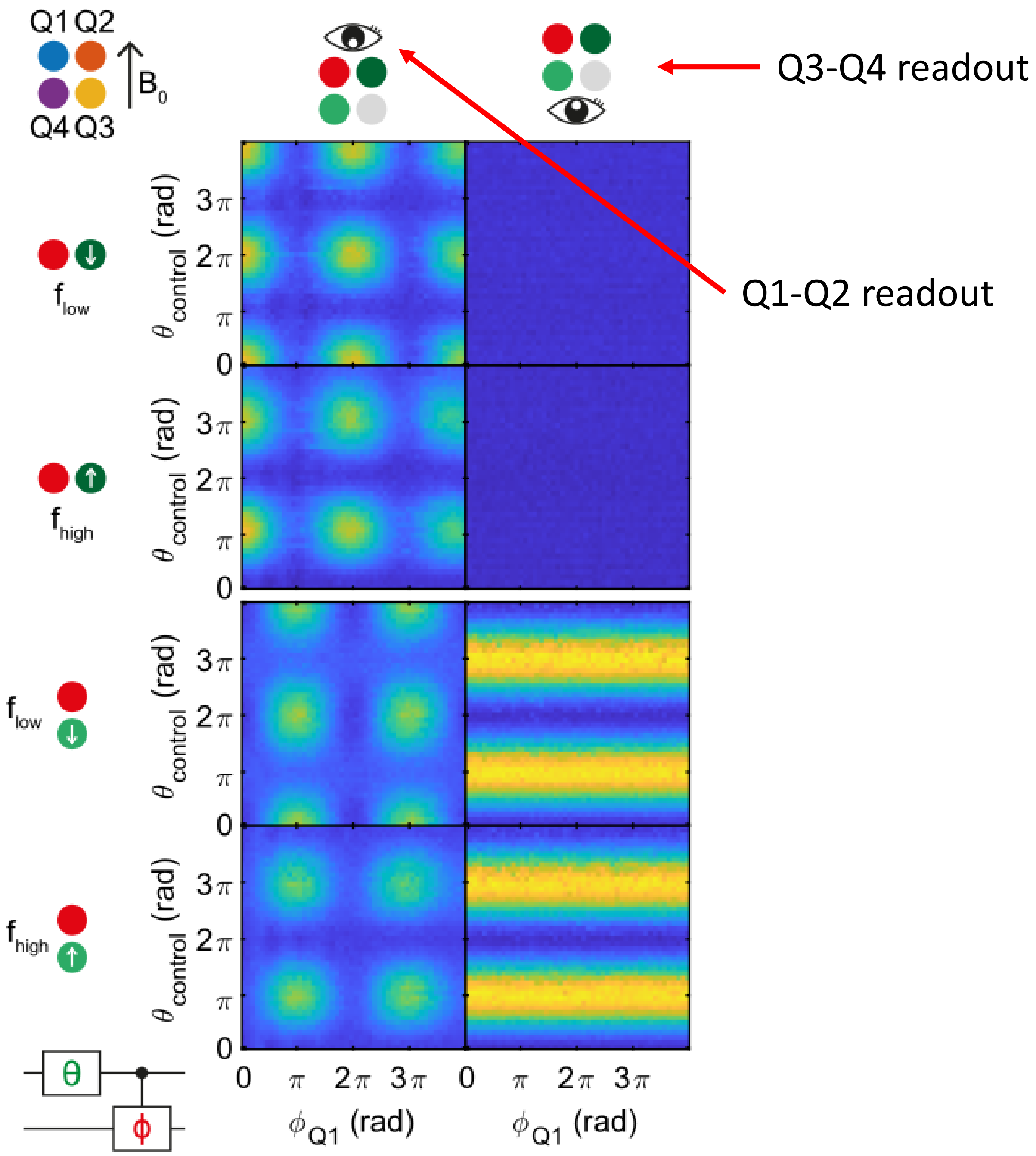




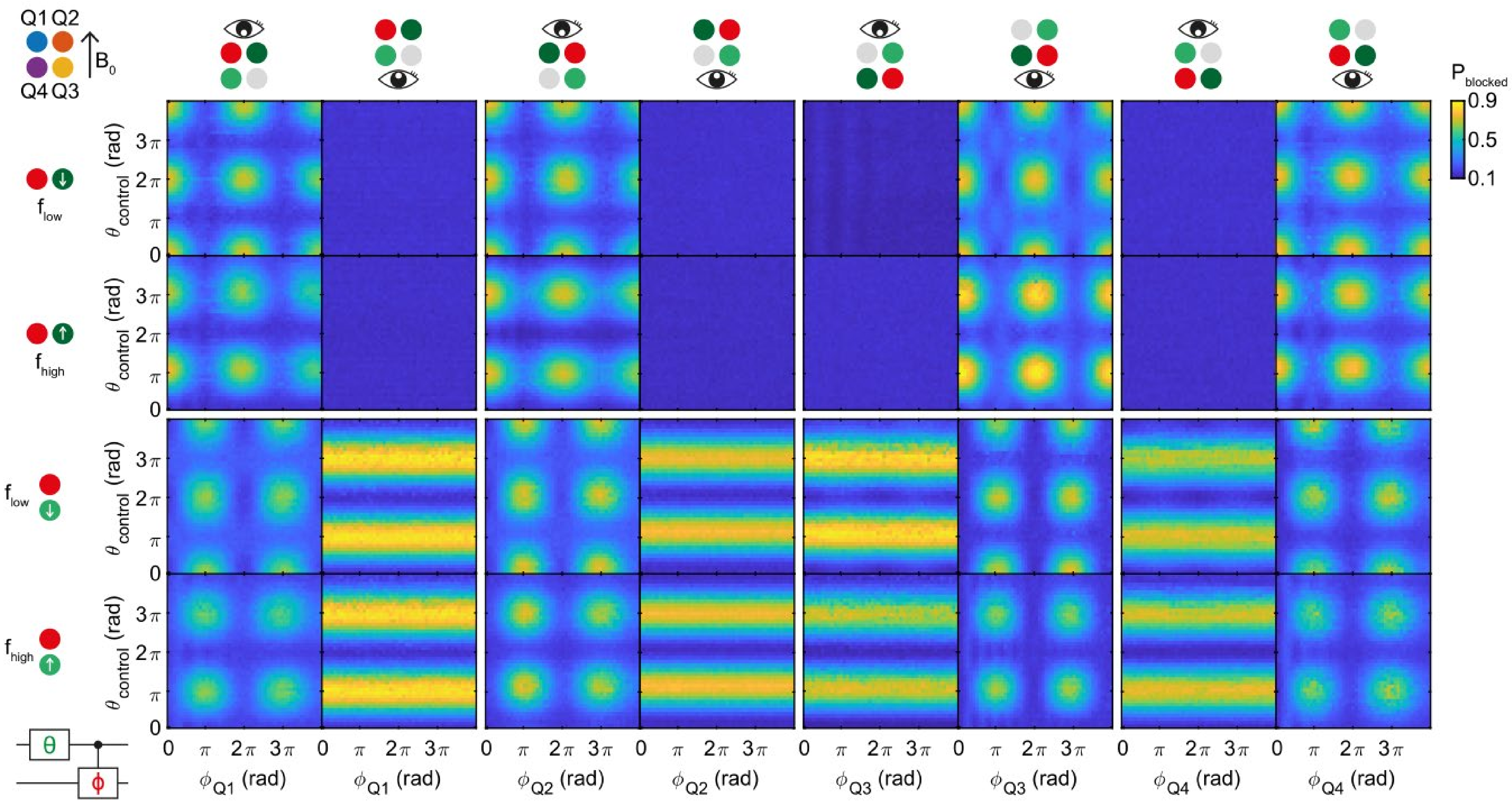


Q2 as control qubit

Q4 as control qubit



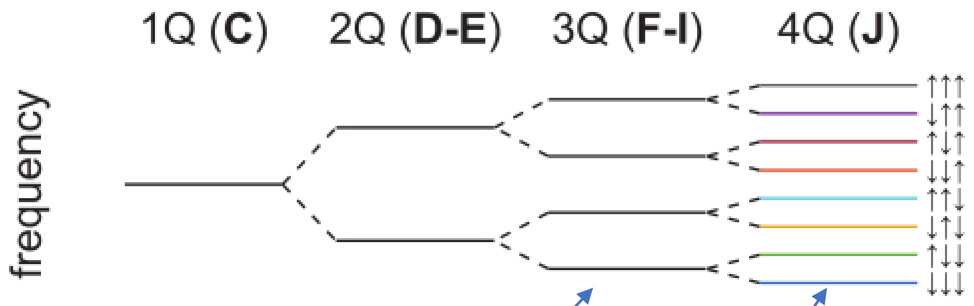
Q1 Q2
B0
Q4 Q3
Q3-Q4 readout
Q1-Q2 readout
f_low
f_high
f_low
f_high
θ_control (rad)
0 π 2π 3π
θ
ϕ
ϕ_Q1 (rad)

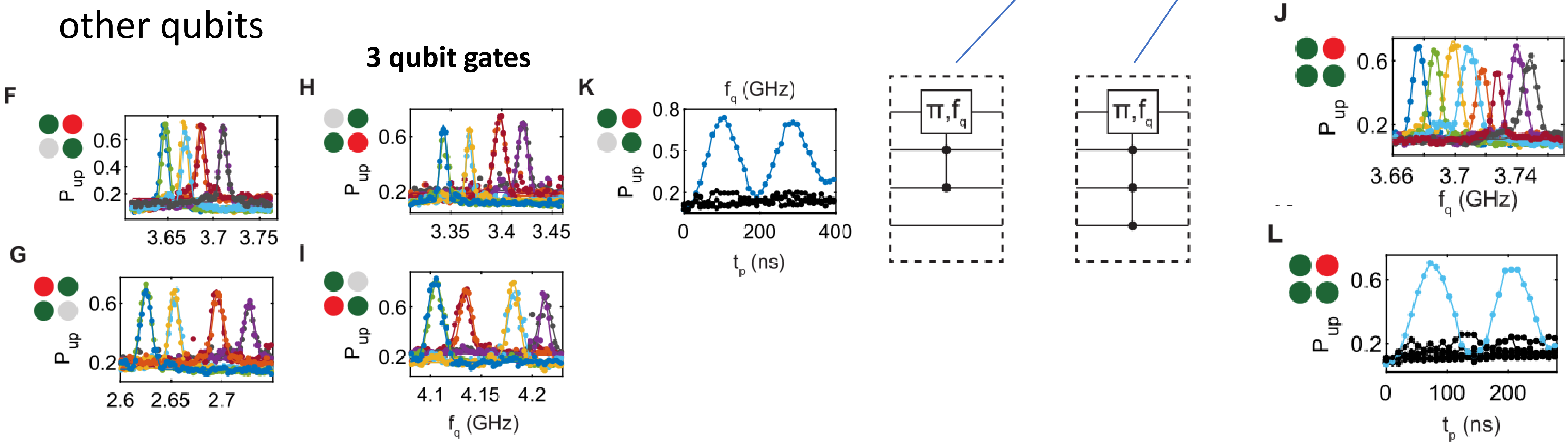


Q1 Q2
Q4 Q3
B_0
$P_{blocked}$
0.9
0.5
0.1
f_{low}
f_{high}
f_{low}
f_{high}
$\theta_{control}$ (rad)
0
π
2π
3π
ϕ_{Q1} (rad)
ϕ_{Q1} (rad)
ϕ_{Q2} (rad)
ϕ_{Q2} (rad)
ϕ_{Q3} (rad)
ϕ_{Q3} (rad)
ϕ_{Q4} (rad)
ϕ_{Q4} (rad)
θ
ϕ

3 and 4-qubit gates: CROT

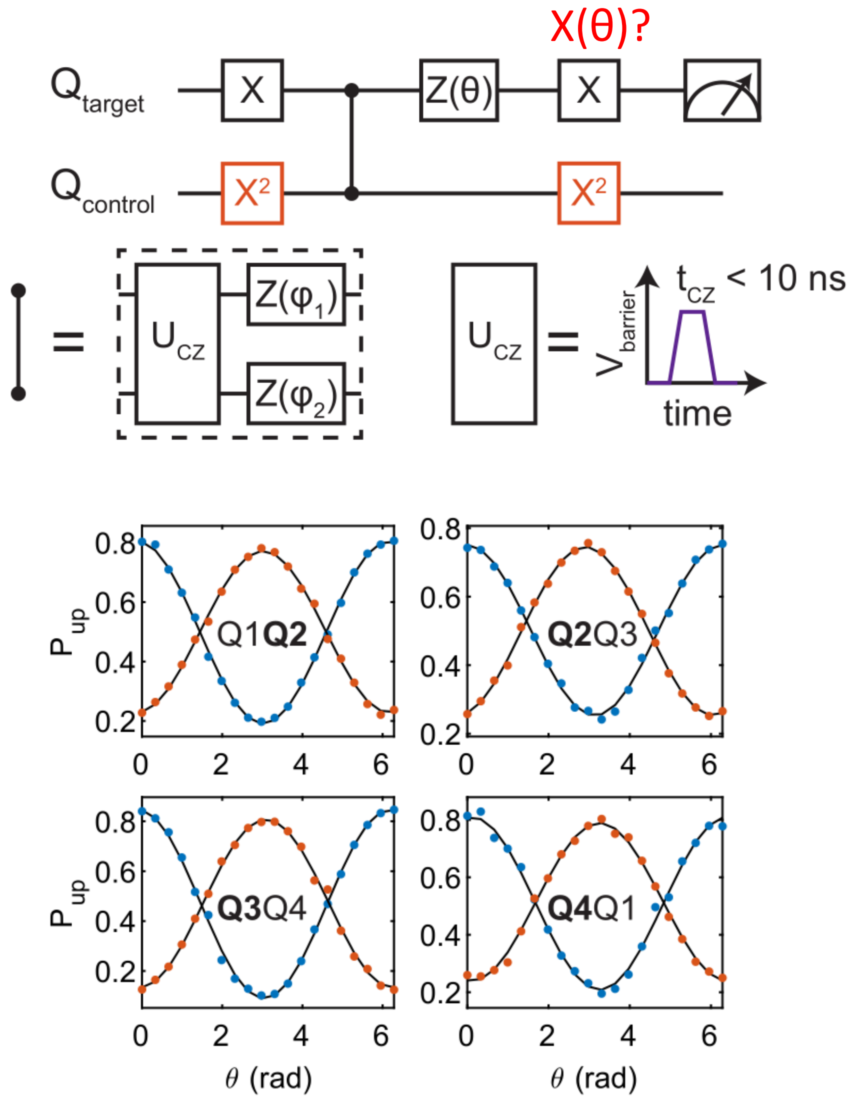
- turn on exchange interaction of 3 or 4 qubits
- rotation of a qubit can now depend on state of 2 or 3 other qubits





2-qubit gates: CPHASE

- increasing **exchange interaction** (pulse barrier voltage) causes energy shift of P and AP states
- energy shift -> detuning -> conditional rotation around z
- **CPHASE** = voltage pulse U_{CZ} + virtual single qubit Z gates
- CZ gate in 10ns



control qubit – **target qubit**

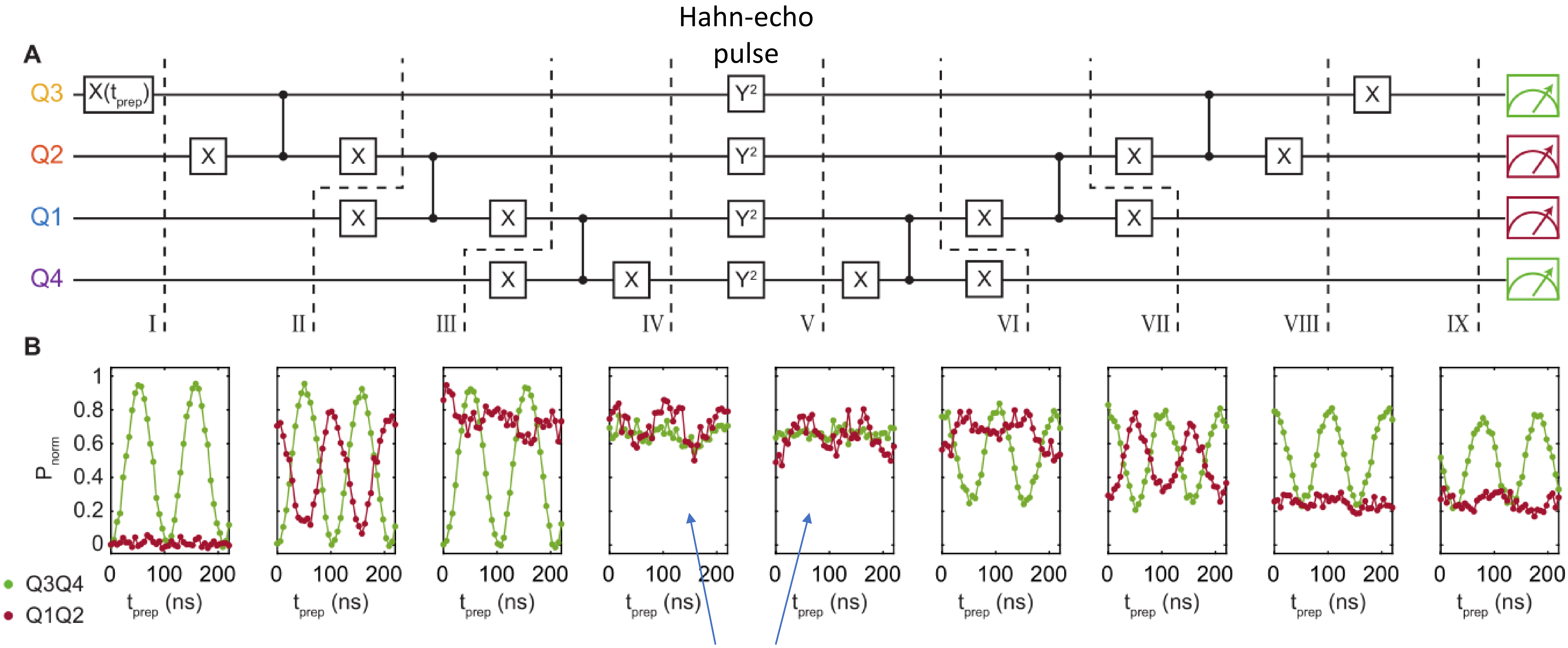
GHZ state generation

- generating a 4-qubit Greenberger-Horne-Zeilinger state
- GHZ is **maximally entangled** state
- extend maximum operation time by integrating dynamical decoupling

example of a 3-qubit GHZ state

$$|\mathrm{GHZ}\rangle = \frac{|000\rangle + |111\rangle}{\sqrt{2}}$$

GHZ state generation



oscillations between |↑↓↑↓⟩ and |↓↑↓↑⟩ not visible in parity readout

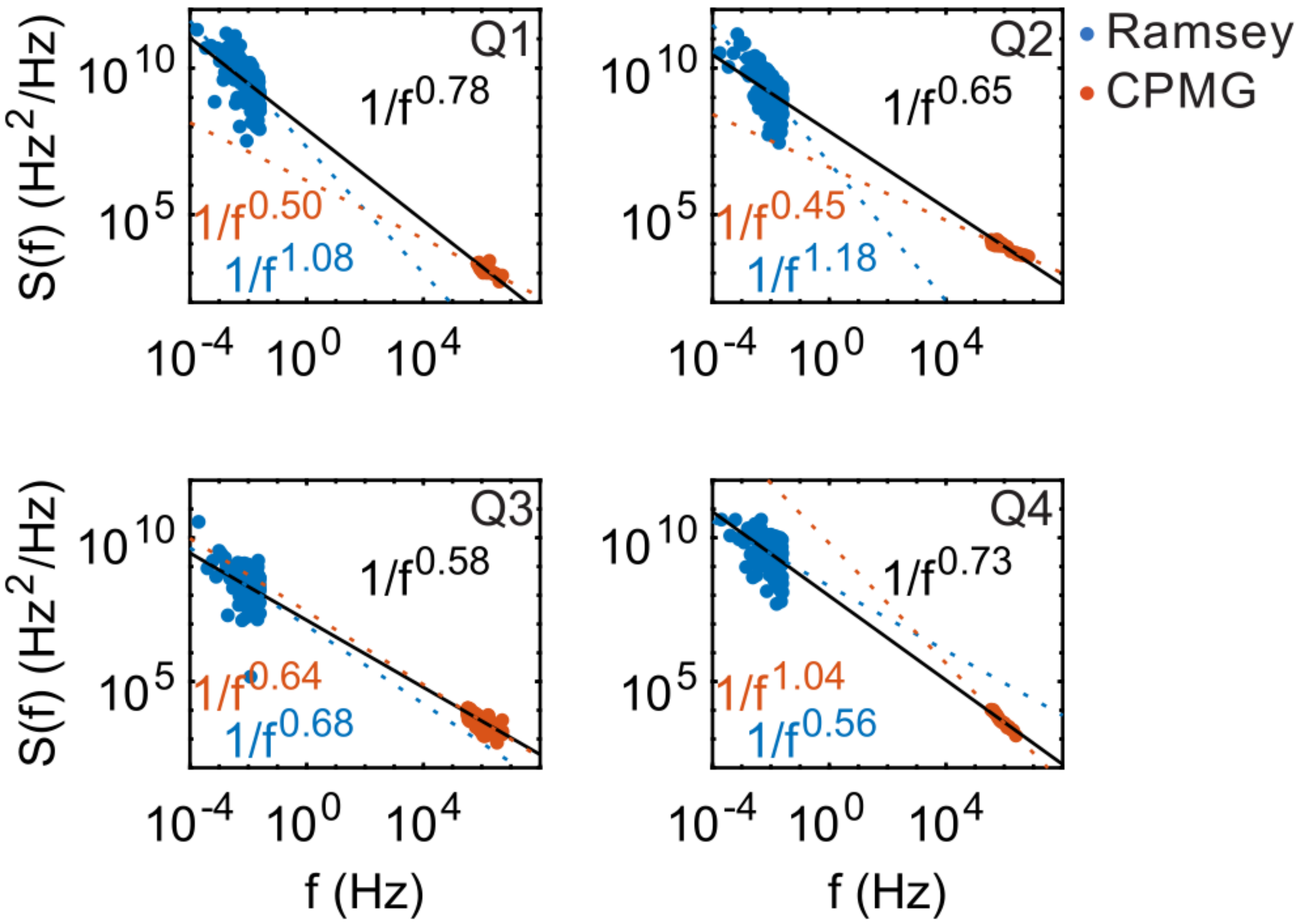
Conclusion

- 2-by-2 array of Ge QDs with tunable nearest-neighbour coulping
- latched parity readout using RF charge sensors
- 4 qubits with long coherence (T2* ~ 230ns) and high fidelity (~99.7%)
- 2-qubit CX (100ns) and CZ (10ns) gates
- 3- and 4-qubit CX gate
- generation of maximally entangled 4-qubit state

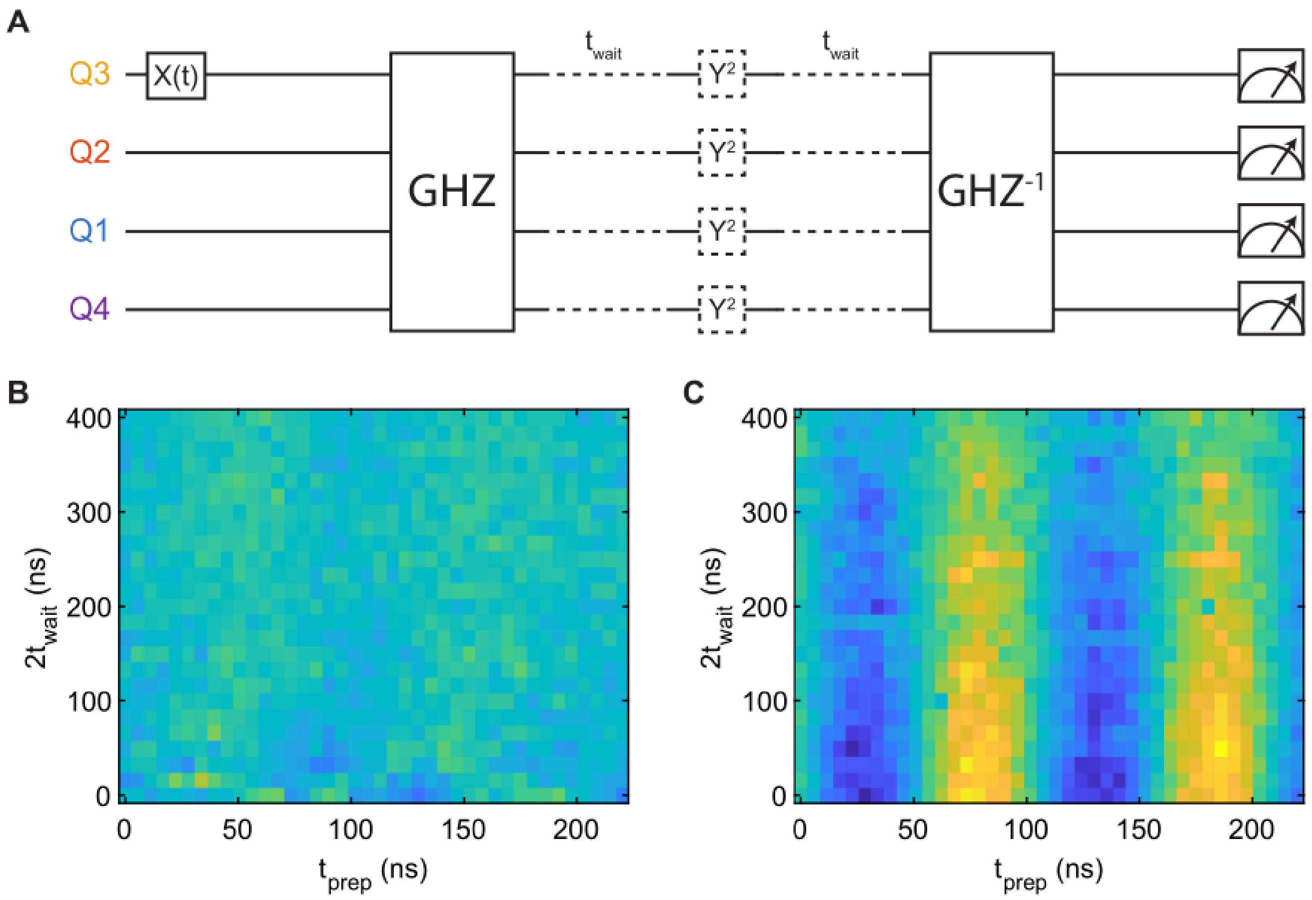
Appendix

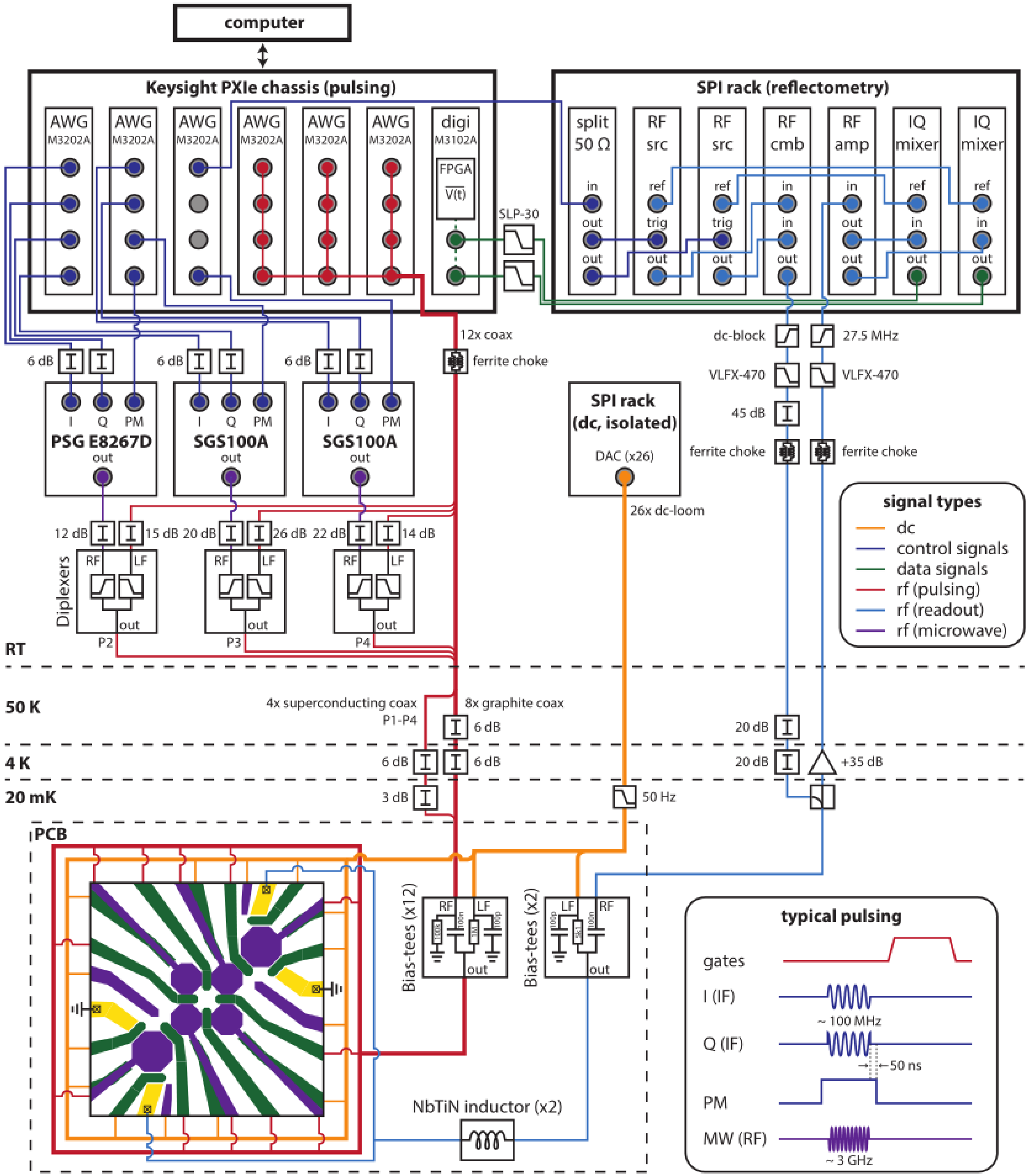
Noise analysis

- possible noise sources: nuclear spins (unpurified Ge) and charge noise



GHZ without dynamical decoupling




computer
Keysight PXIe chassis (pulsing)
AWG M3202A
digi M3102A
FPGA
V(t)
SLP-30
SPI rack (reflectometry)
split 50 Ω
RF src
RF cmb
RF amp
IQ mixer
ref
trig
in
out
12x coax
ferrite choke
6 dB
I Q PM
PSG E8267D
SGS100A
out
SPI rack (dc, isolated)
DAC (x26)
26x dc-loom
dc-block
27.5 MHz
VLFX-470
45 dB
signal types
dc
control signals
data signals
rf (pulsing)
rf (readout)
rf (microwave)
12 dB 15 dB 20 dB 26 dB 22 dB 14 dB
Diplexers
RF LF
P2 P3 P4
RT
50 K
4x superconducting coax P1-P4
8x graphite coax
20 dB
4 K
+35 dB
20 mK
3 dB
50 Hz
PCB
Bias-tees (x12)
Bias-tees (x2)
NbTiN inductor (x2)
typical pulsing
gates
I (IF)
~ 100 MHz
Q (IF)
50 ns
PM
MW (RF)
~ 3 GHz