A new FDSOI spin qubit platform with 40nm effective control pitch

T. Bédécarrats[1], B. Cardoso Paz[2], B. Martinez Diaz[3], H. Niebojewski[1], B. Bertrand[1] , N. Rambal[1], C. Comboroure[1], A. Sarrazin[1], F. Boulard[1], E. Guyez[1], J.-M. Hartmann[1], Y. Morand[1], A. Magalhaes-Lucas[1], E. Nowak[1], E. Catapano[1], M. Cassé[1], M. Urdampilleta[2], Y.-M. Niquet[3], F. Gaillard[1], S. De Franceschi[3], T. Meunier[2], M. Vinet[1]

Université Grenoble Alpes and [1] CEA-Leti, [2] CNRS Institut Néel, [3] CEA-Irig, F-38000 Grenoble, France

presented by Simon Geyer

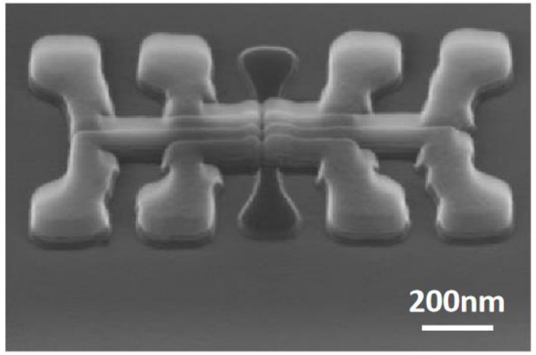
8/8/2022

Contents

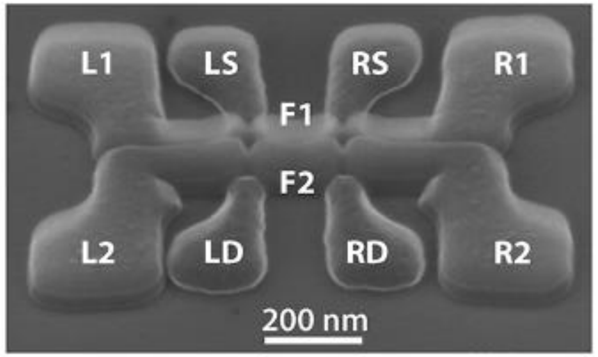
- state-of-the-art
- simulations
- fabrication
- RT characterization
- low-T characterization

State-of-the-art FDSOI platform

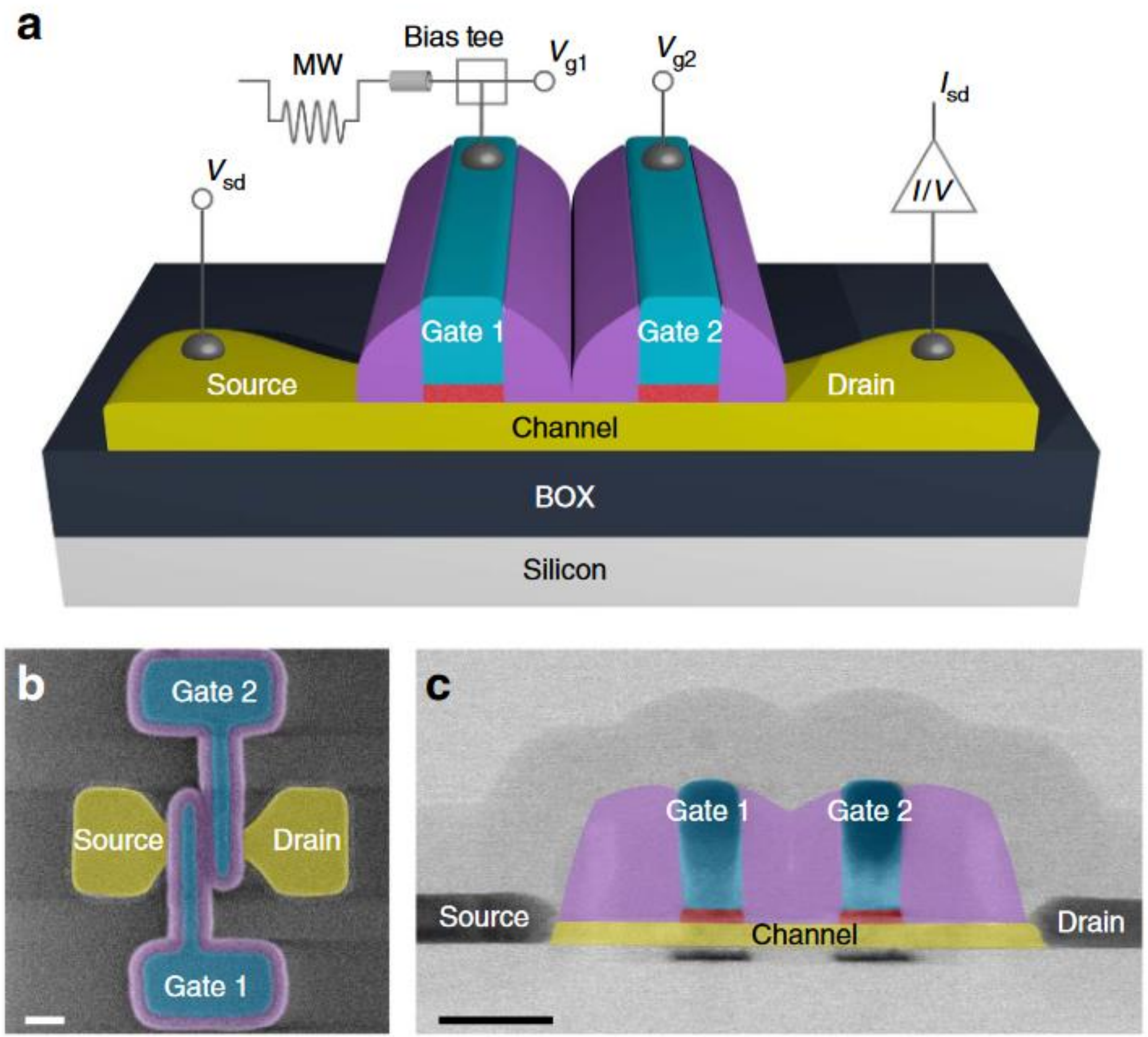
- 300mm process with immersion-DUV litho
- linear chain of electron/hole qubits
- 2xN arrays of QDs (face-to-face gates)
- natural barriers by self-aligned spacers
- global top- and back-gate
- high-temperature single-shot spin readout (PSB)
- single-shot qubit readout (Elzerman)



Hutin *et al.*, IWDM 2019



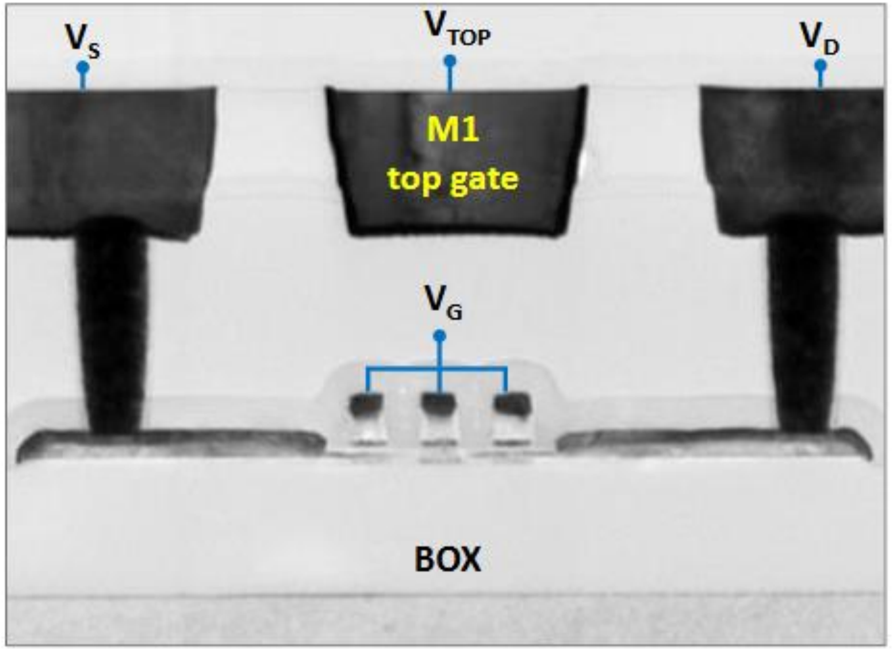
Duan *et al.*, Nano Lett. 2020

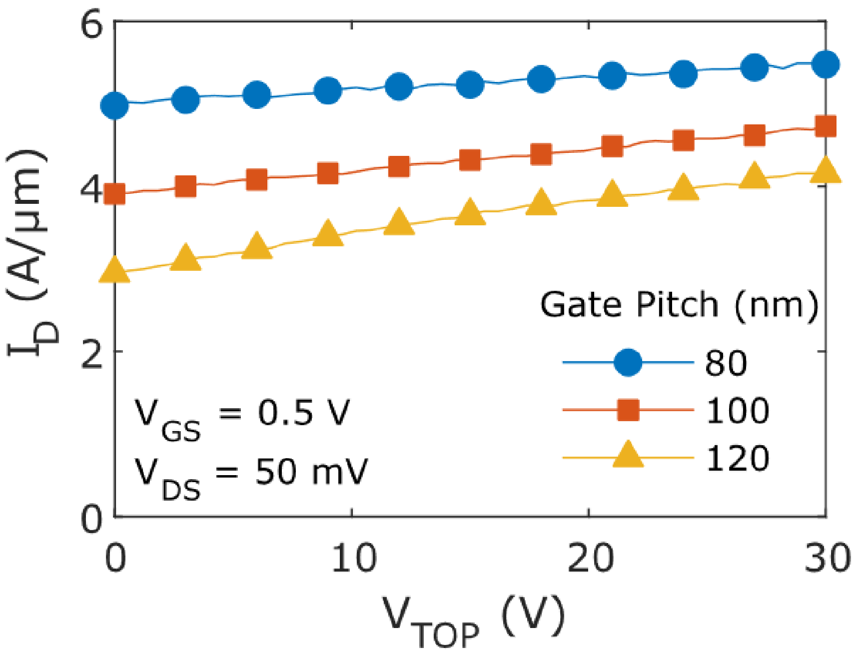


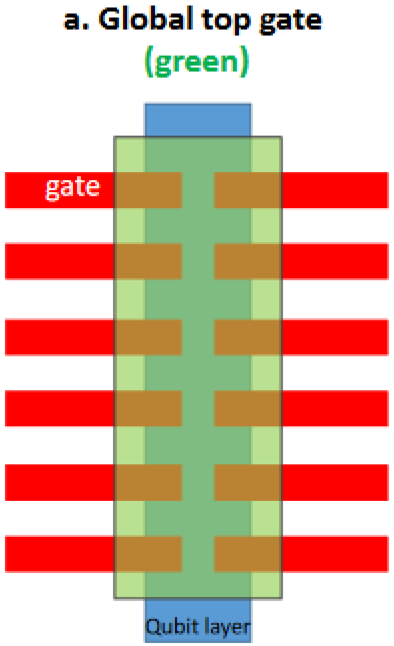
Maurand *et al.*, Nat. Comm. 2016

State-of-the-art FDSOI platform

- problem: no control over tunnel barriers if each gate accumulates one QD

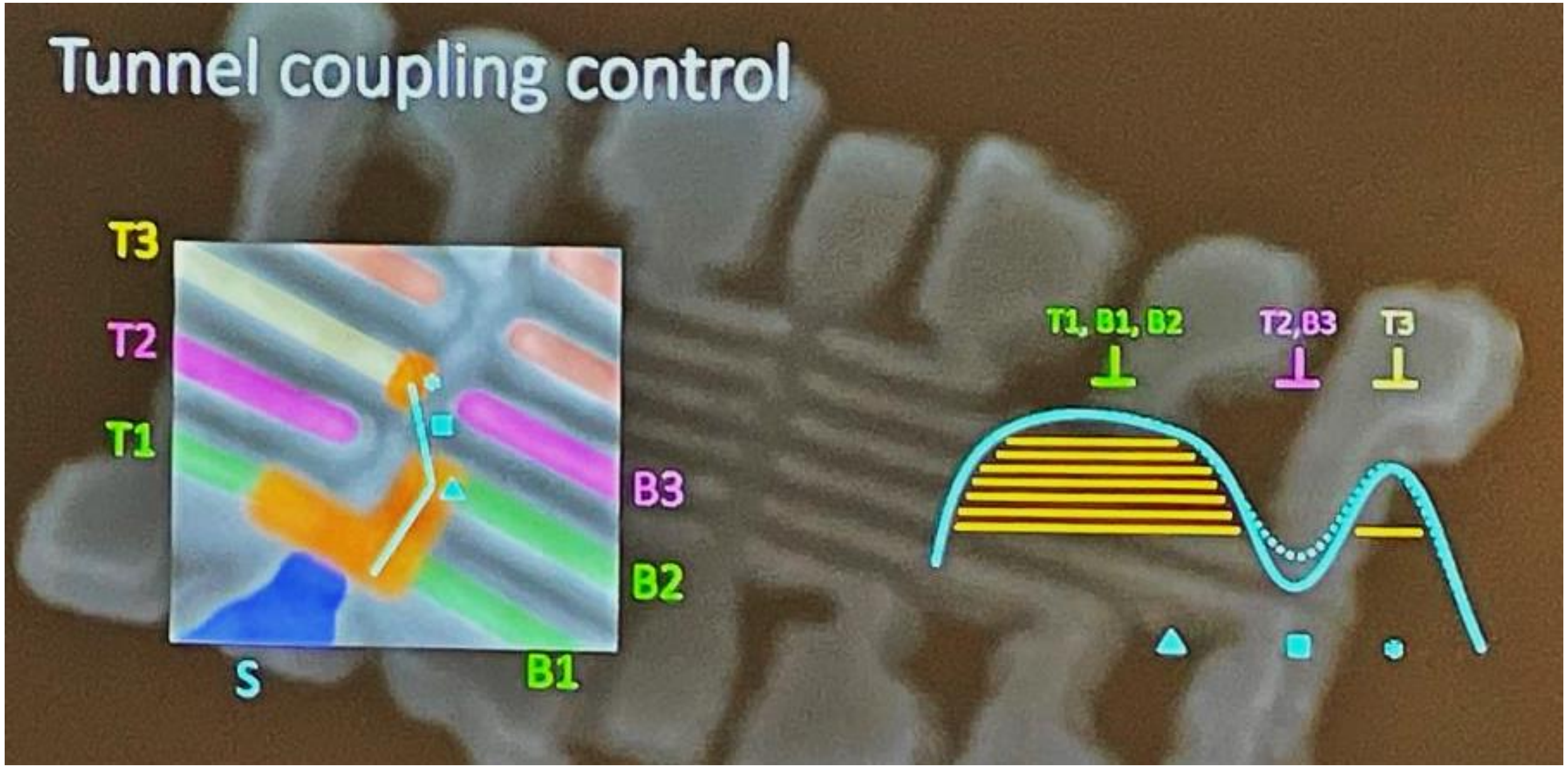




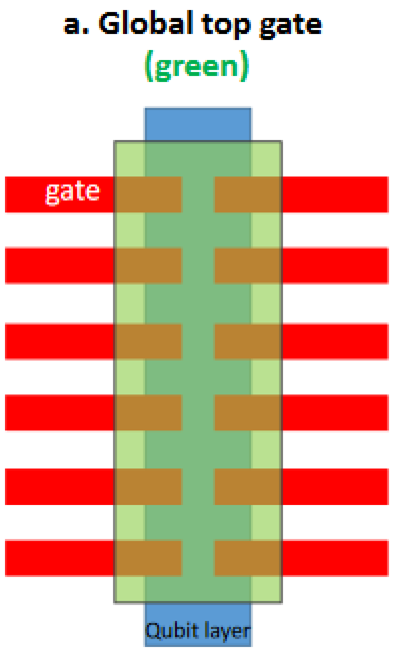


State-of-the-art FDSOI platform

- problem: large QDs needed for scheme with QD below every second gate -> no quibts

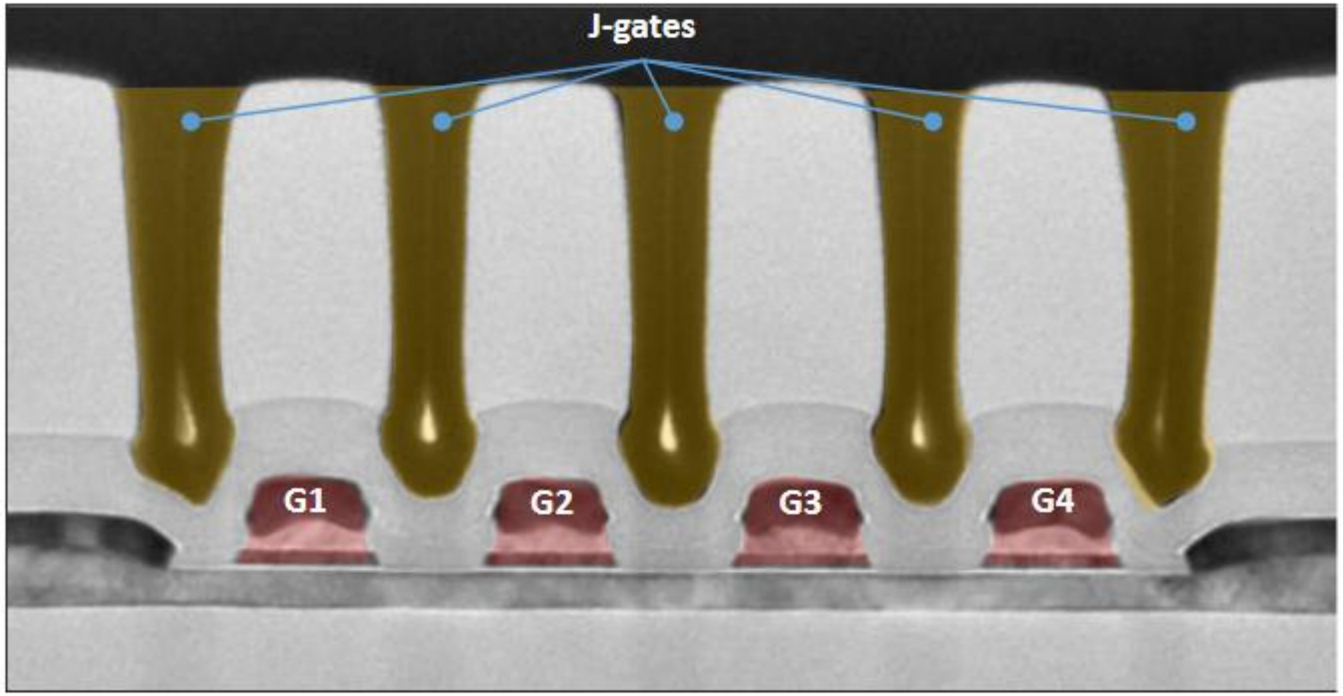


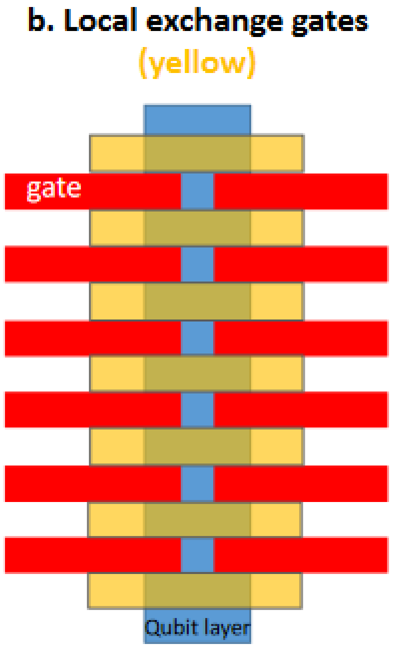
Vivien Schmitt, APS march meeting 2022



New FDSOI platform

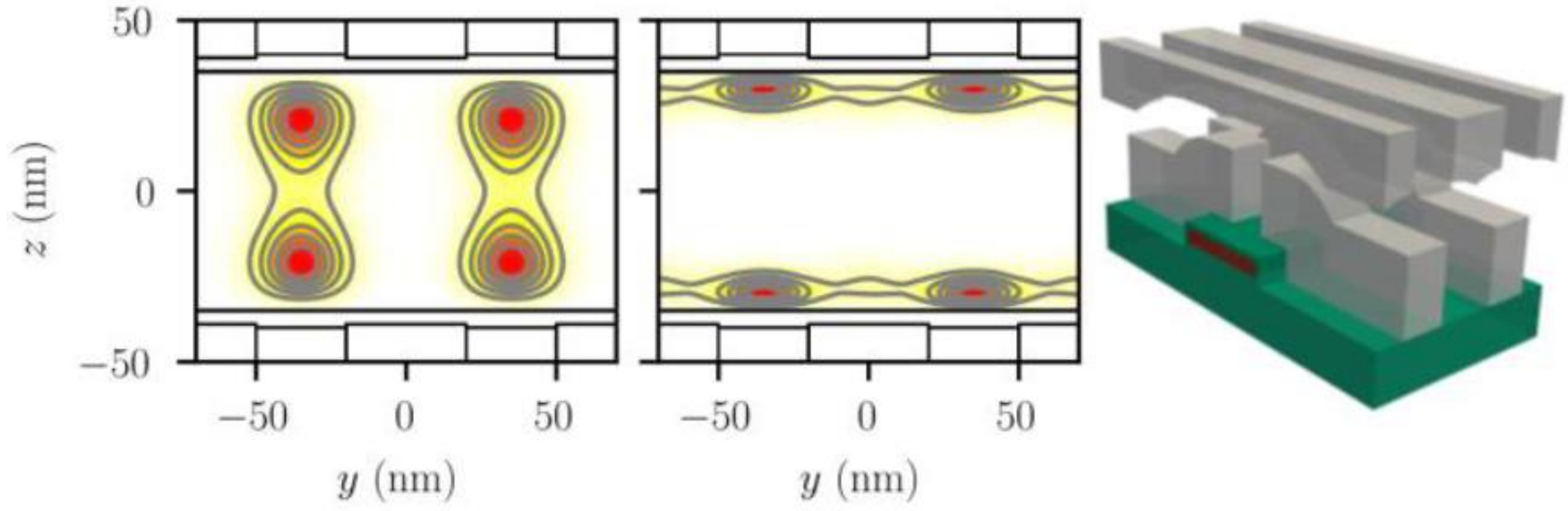
- Solution: local exchange gates (J-gates)

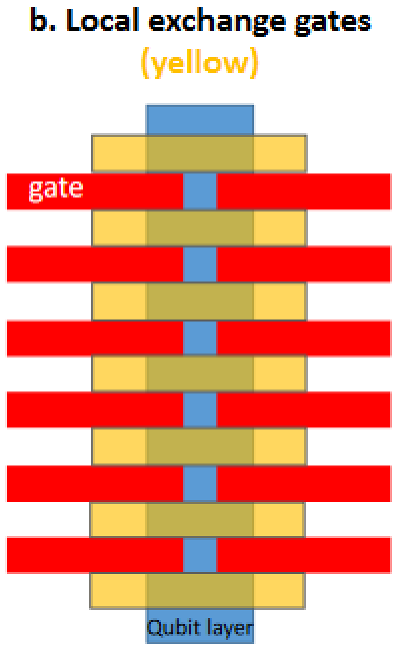




Simulations

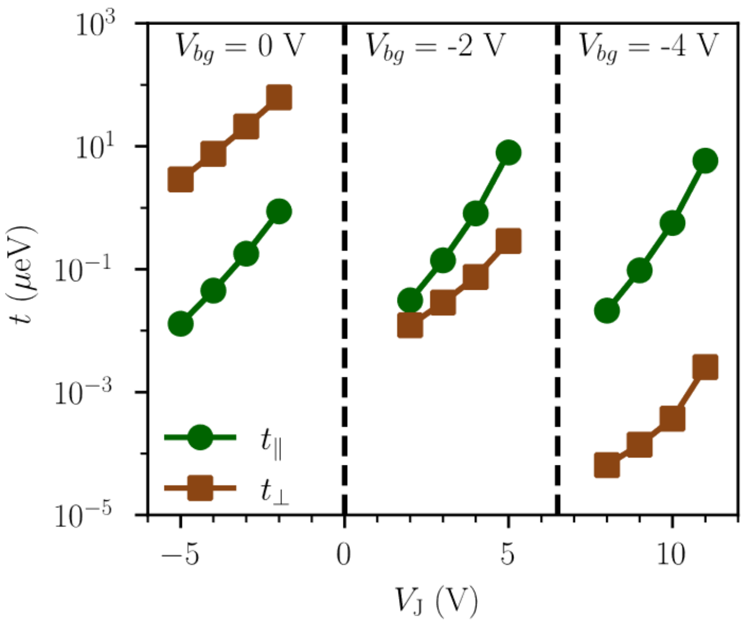
- Poisson + effective mass simulation
- periodic structure of 2xN array
- two modes:
  - face-to-face coupling (readout)
  - longitudinal coupling (2-qubit gates)



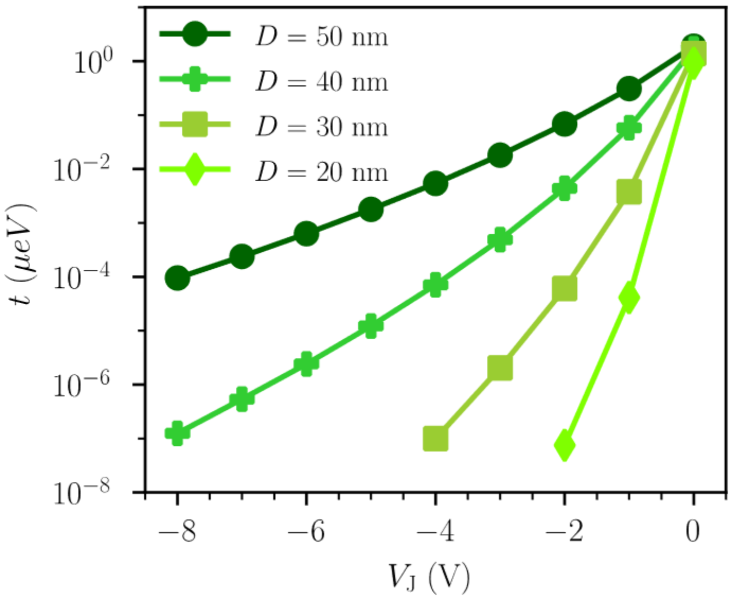


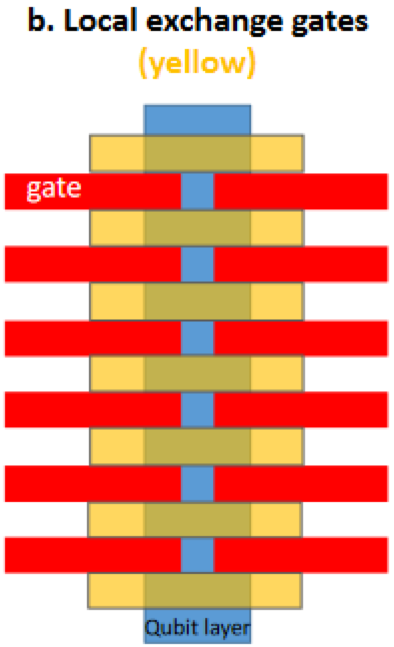
Simulations

- Poisson + effective mass simulation
- periodic structure of 2xN array
- two modes:
  - face-to-face coupling (readout)
  - longitudinal coupling (2-qubit gates)



D = first gate layer thickness

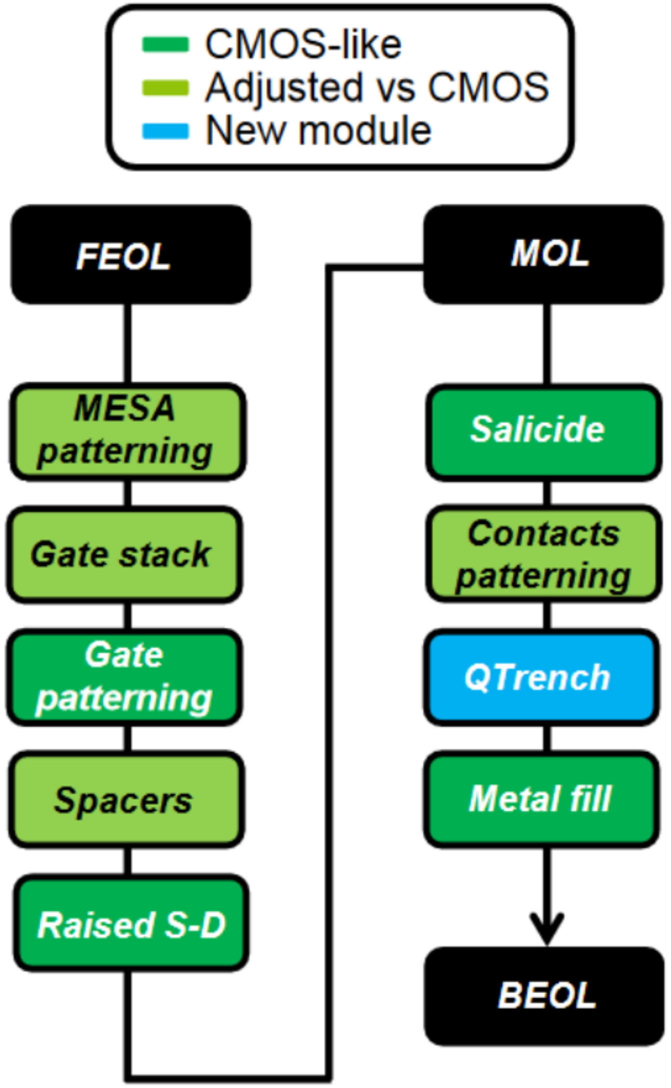




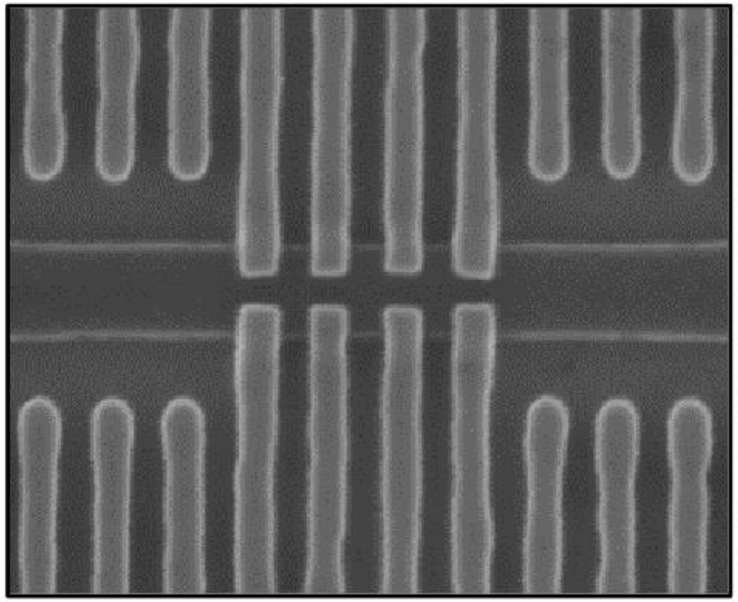
→ simulation shows more control than with global top gate

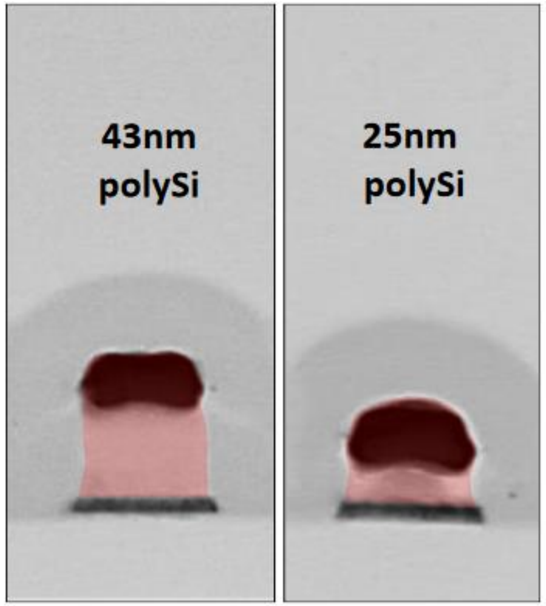
Fabrication

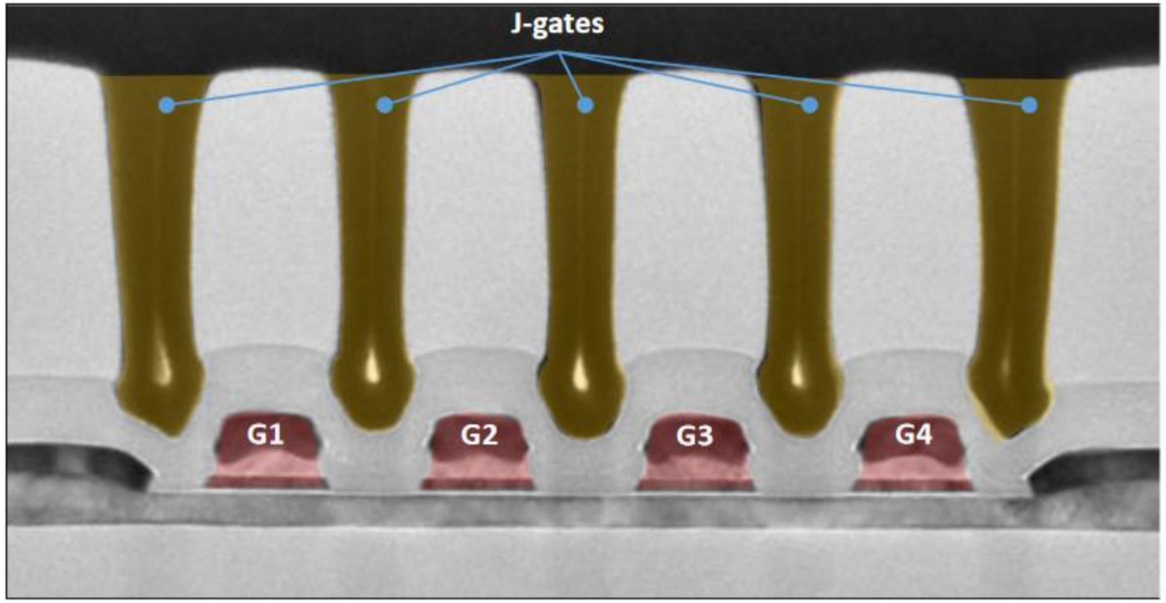
- 300mm wafer scale using 193nm immersion DUV
- mesa: ~20nm Si, BOx: 145nm
- gate stack:
  - 2.5nm SiO_2 + high-k?
  - ~7nm TiN / 25nm polySi
- gate pitch: 80nm
- spacer: 25(?)nm SiN
- contacts
  - epitaxial growth: Si:P or SiGe:B
  - NiPt silicidation
- E-beam litho: trenches for J-gates (material?)
- effective pitch: 40nm



Fabrication

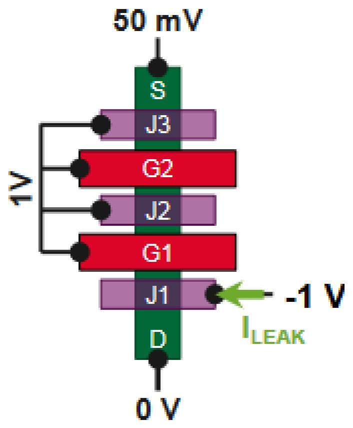


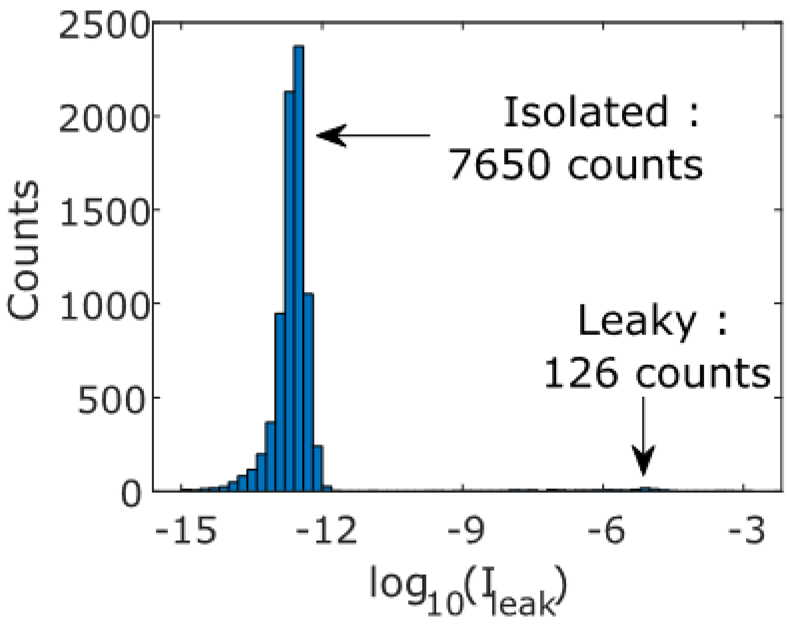




RT characterization

- from now on: only 1D arrays of electron QDs
- mass test of 2500 DQD devices (2 plunger+ 3 J-gates)
- 98.3% yield in leakage test of J1





RT characterization 2

- 90nm pitch devices
- select 79 out of 384 4-QD devices that work nicely (4 plunger + 5 J-gates)
- → yield 21%
- test variability in G1-G4 (old gate layer)

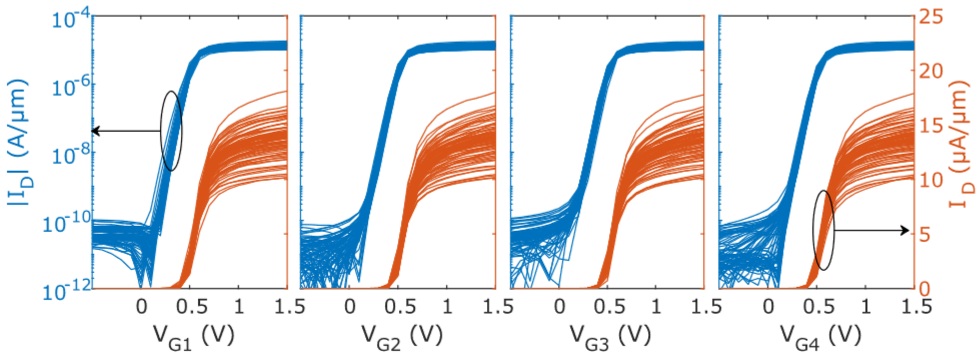
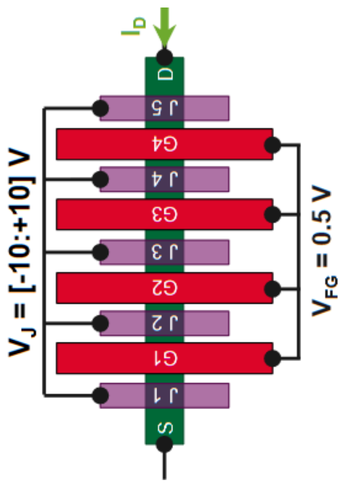
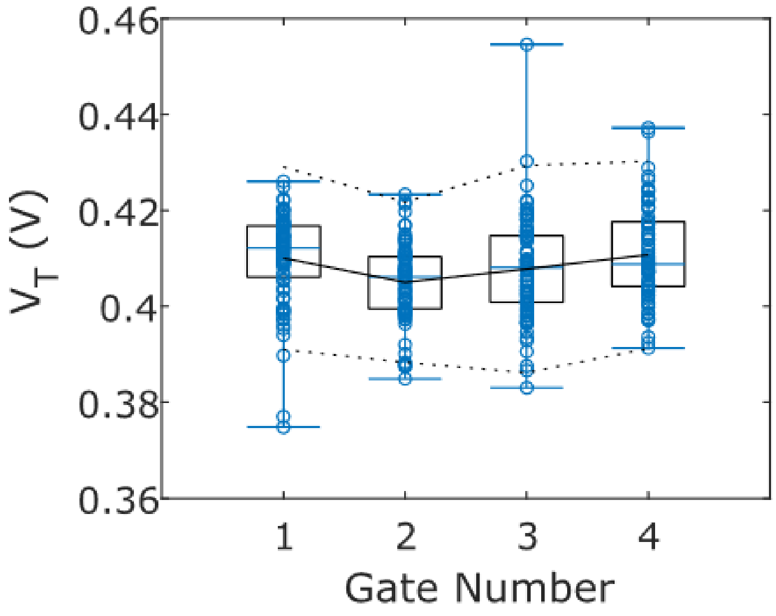
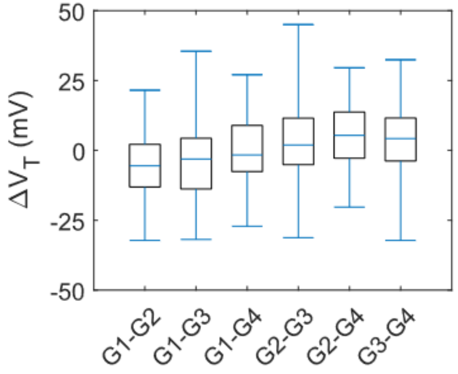
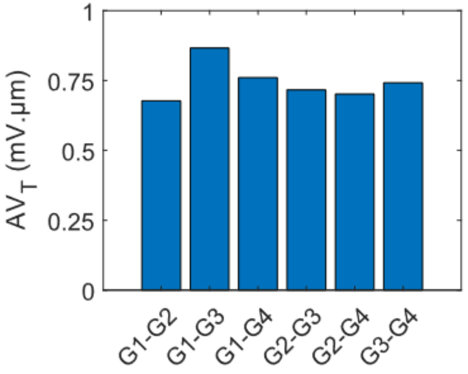


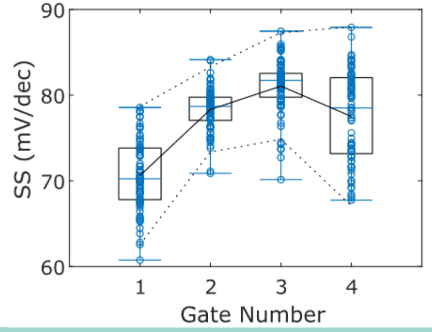
Fig. 12: in logaritmic scale (blue curves, left axis) and linear scale (orange curves, right axis) Drain current I_D versus gate voltage V_G curves for 79 functional 4-QDs in series, at V_{DS} = 50 mV, an unsewpt serie gate bias of 1.5 V and J-gates set to 0V. (functionality criteria : all gates must have $I_{D,max}$ > 10 µA/µm, $I_{D,min}$ < 10 pA/µm, $I_{G,max}$ <10pA/µm and $V_T \in$ [0.3; 0.48] V).







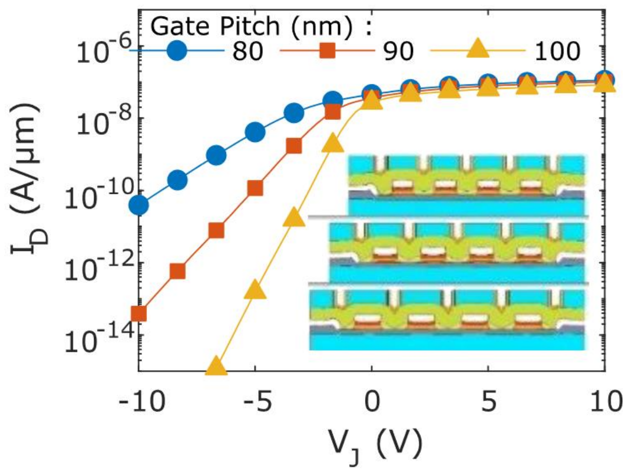


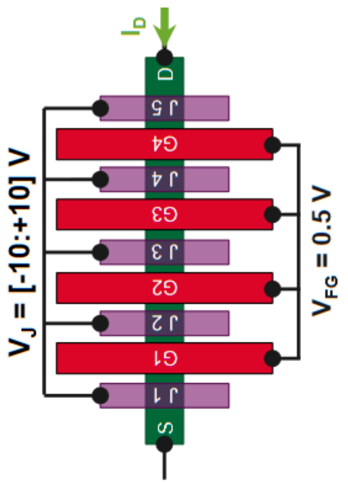


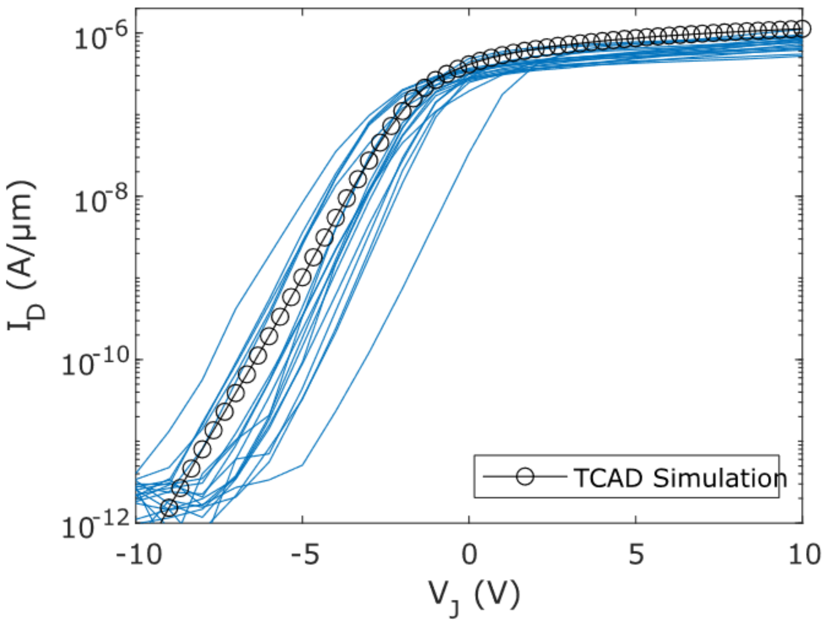
RT characterization 3

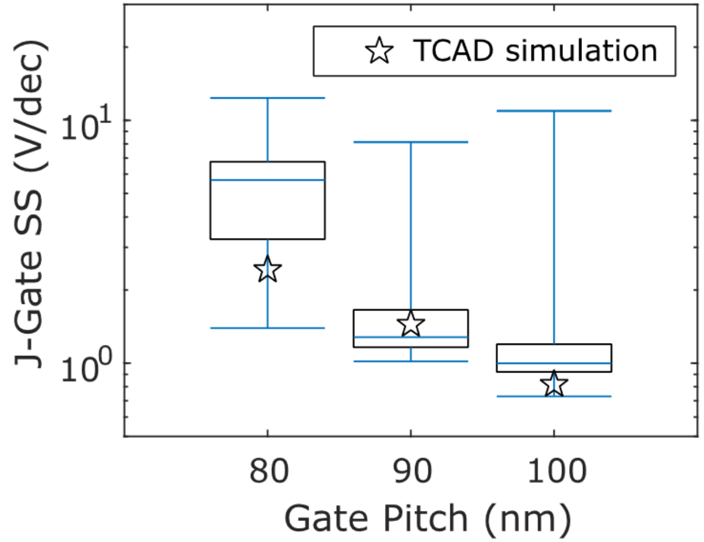
- test variability in J (new gate layer)
- all J-gates shorted
- gate pitch 80, 90 and 100nm

TCAD:



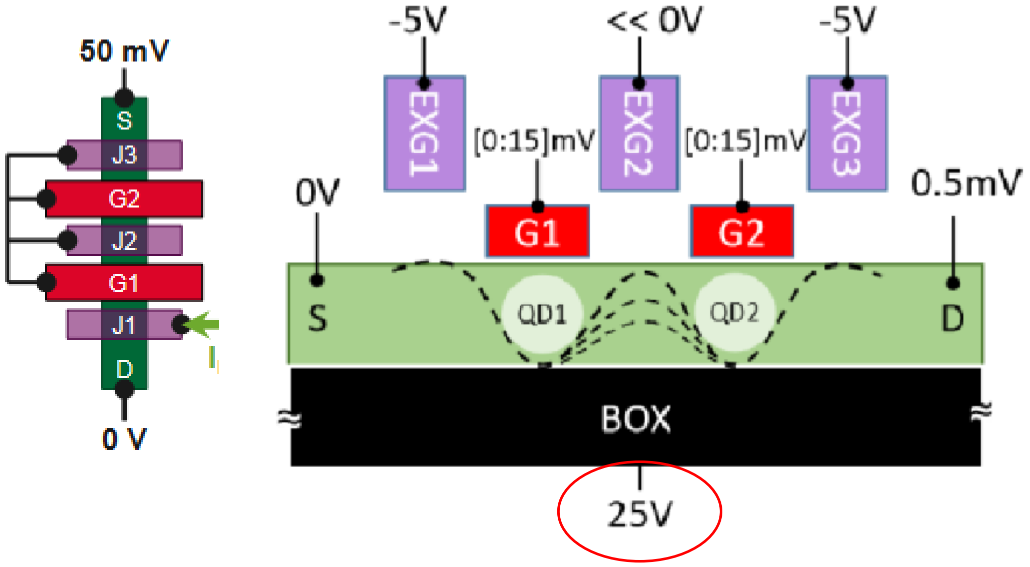


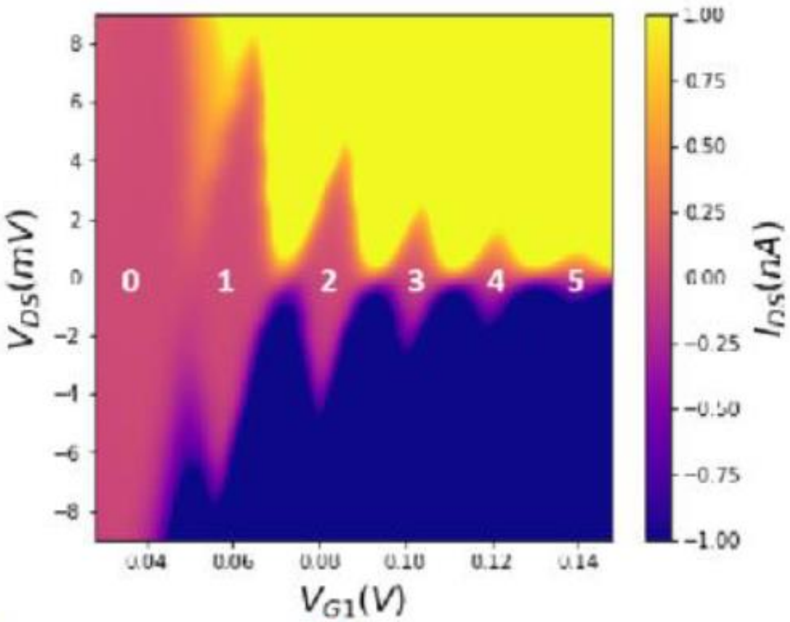


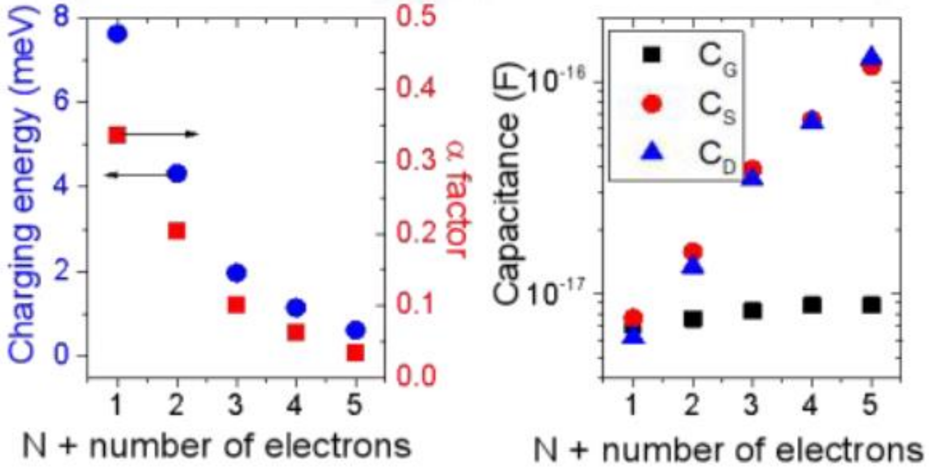


Low-T characterization: QD

- back to DQD devices (2 plunger+ 3 J-gates) at 4.2 K
- back gate +25V to push QD to back interface
- operate as single QD



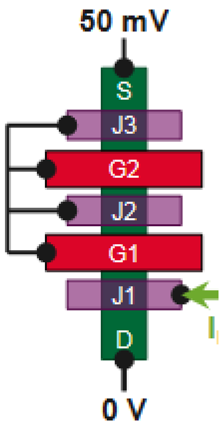


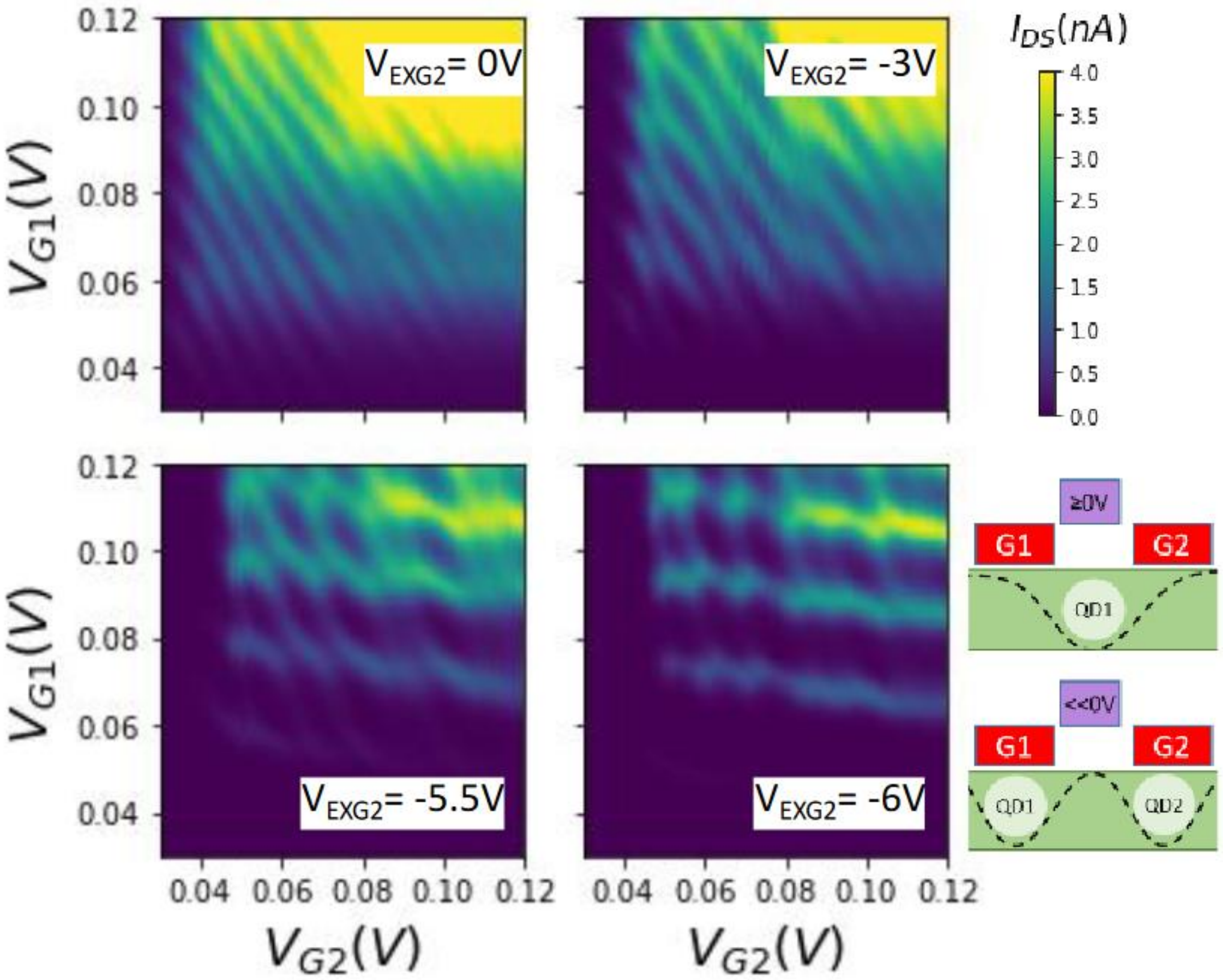


simon.geyer@unibas.ch

Low-T characterization: DQD

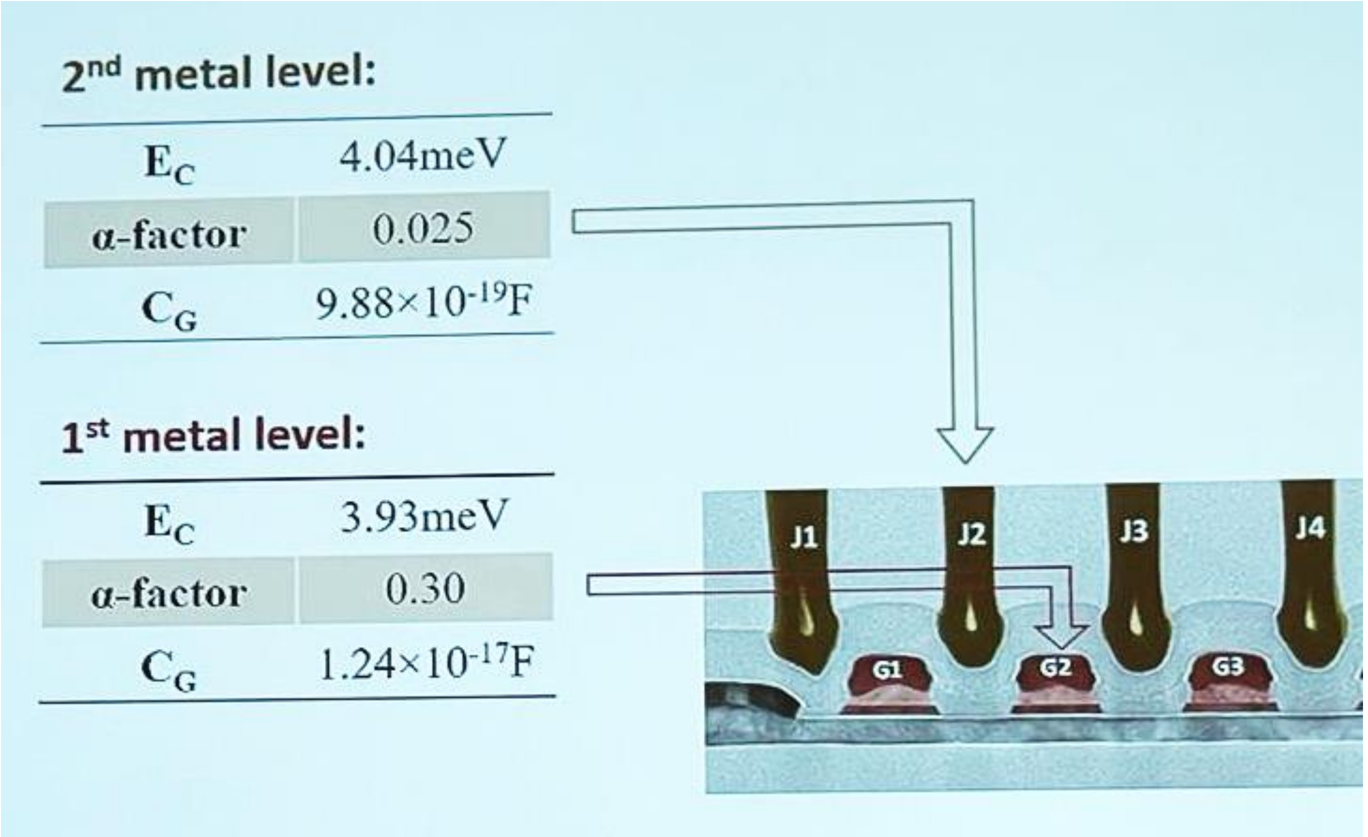
- tune from single QD to DQD using J-gate voltage





Role of gates

- Is switching the role of P and J-gates beneficial?



Bruna Paz, APS march meeting 2022

Conclusion

- new device layout with 40nm pitch
- simulations predict subthreshold slope and tunneling rates
- RT characterization shows good yield for DQD devices and small variability for pre-selected sample of 4QD devices
- 4K characterization shows control over tunnel coupling of neighboring QDs
- quantitative study of tunneling rates vs V_J is to be shown