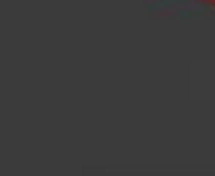
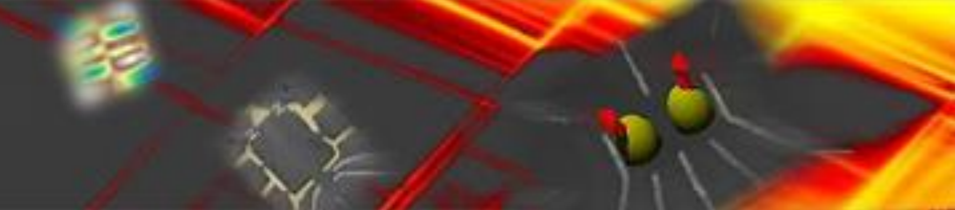

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Effect of surface treatments on ALD Al_2O_3/4H-SiC metal–oxide–semiconductor field-effect transistors

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13.08.2021

Motivation

- 4H-SiC enables
  - to operate at high power and high temperature
  - fast switching applications
- Performance limited by interfacial defects
- So far
  - post-oxidation annealing in nitrogen and
  - Boron or phosphorus involving
- Alternative approach: deposited dielectrics (e.g. Al_2O_3)
  - High dielectric constant (k = 7 – 10 for Al_2O_3)
  - Large band gap (~ 9 eV for Al_2O_3)
  - High conduction band offset (~ 1,7 eV for Al_2O_3 with 4H-SiC)
- This work investigated in the surface treatments prior to atomic layer deposition
  - Improved the electrical quality of the interface and obtained high channel mobility

Fabrication

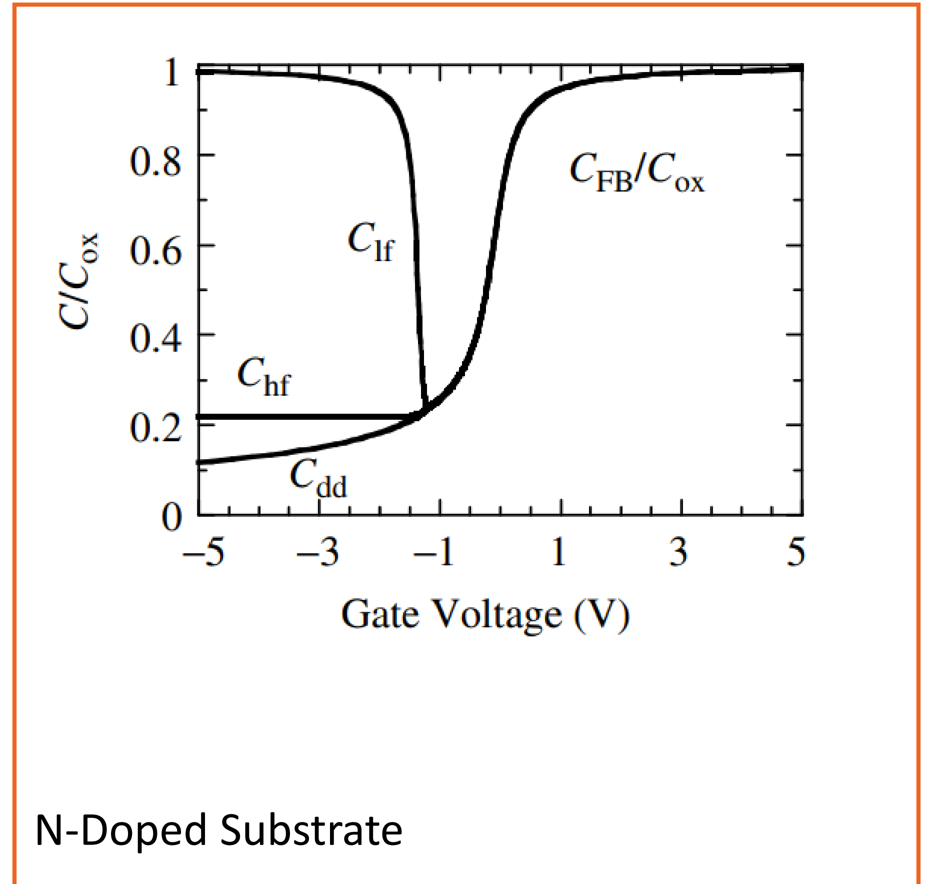
- 4H-SiC
- N-doped ~2 x10^16 / cm^3 (nitrogen)
- 33 nm Al_2O_3 200 °C
- 0,07068 mm^2
- Circular Al gates
  - 100 nm thick
  - 300 µm diameter

- Sacrificial oxidation in O_2: 15 nm thermal oxide completely etched
- Sacrificial oxidation in NO: thermal oxide completely etched
- Sacrificial oxidation in O_2 + H_2 annealing: 15 min, 100 % H_2, 1000 °C, atmospheric pressure
- Sacrificial oxidation in NO + H_2 annealing: 15 min, 100 % H_2, 1000 °C, atmospheric pressure

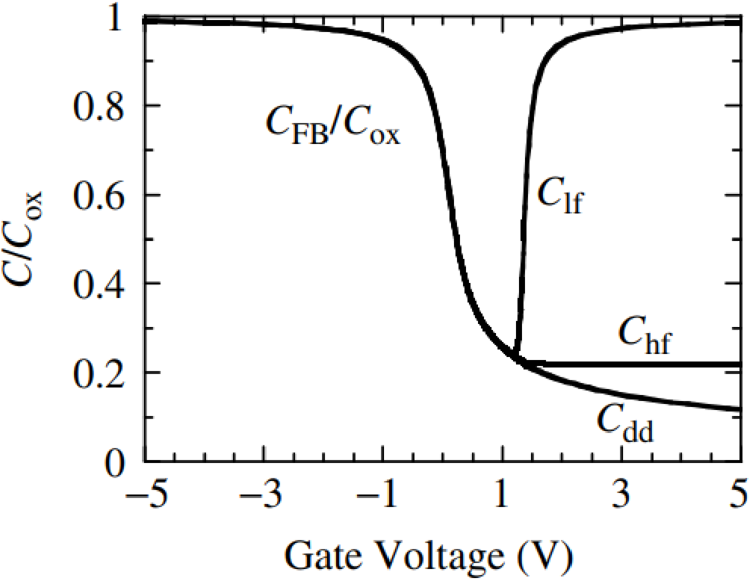
- Silicon
- P-doped ~1 x 10^15 / cm^3
- 24 nm Al_2O_3 225 °C
- 0,09 mm^2 / 0,0225 mm^2 / 0,0064 mm^2
- Quadratic Ti / Pd gates
  - 2 nm / 48 nm thick
  - 300 µm / 150 µm / 80 µm side length

- Native silicon oxide
- Striped native silicon oxide: completely eched

Ideal CV Curves



N-Doped Substrate



P-Doped Substrate

CV Measurements

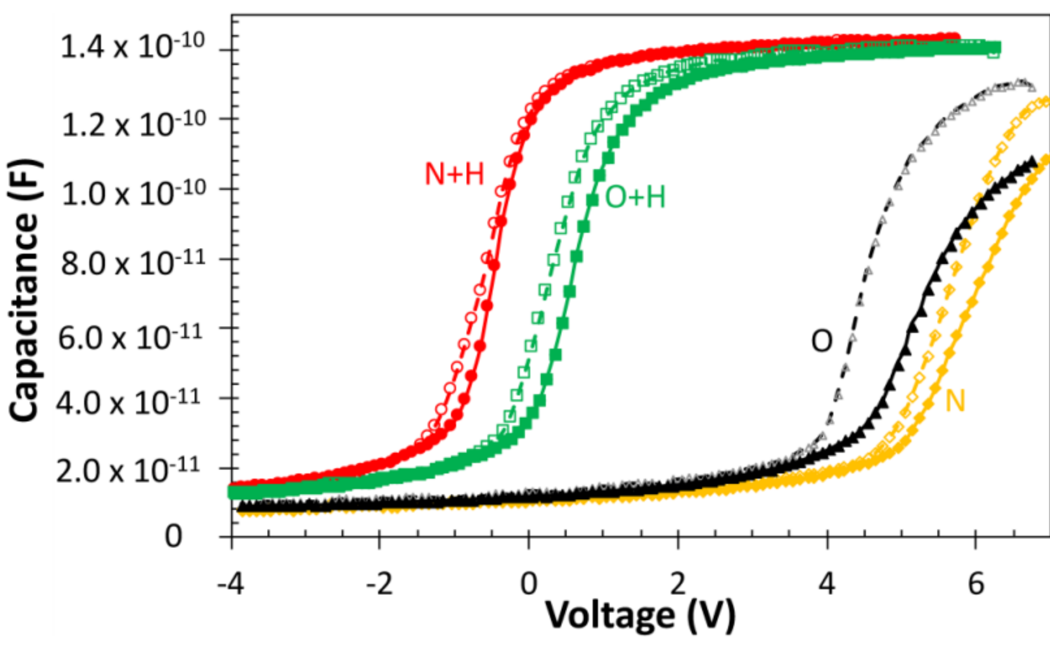
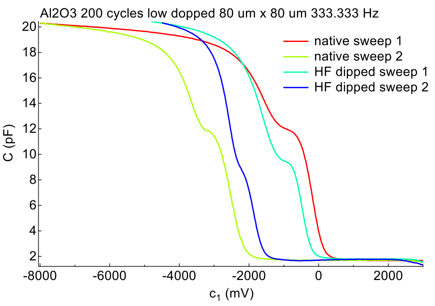


FIG. 1. Typical simultaneous high–low frequency CV characteristics obtained at 298 K for Al_2O_3/4H-SiC MOS capacitors with a gate area of $7.07 \times 10^{-4} cm^2$ prepared with different surface treatments. Solid symbols indicate 100 kHz CV, and hollow symbols indicate quasistatic CV measurements. The labeling of the samples is described in Table I and in the text.



Sweep 1: depletion to accumulation
Sweep 2: accumulation to depletion

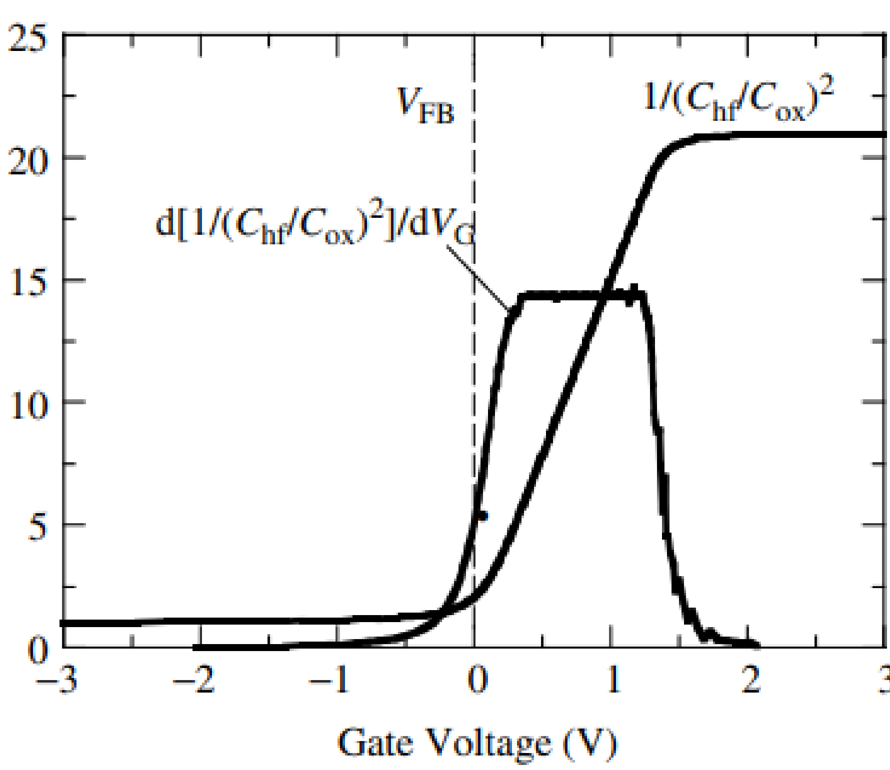
Effective charge densities

TABLE I. Integrated effective interface charge density (N_{eff}) at room temperature under flatband conditions and shallow ($\sim 0.05\ eV \leq E_c - E \leq 0.2\ eV$) interface trap densities (ΔN_{it}) for Al_2O_3/4H-SiC MOS capacitors fabricated with different surface treatment processes as indicated in the text. The sign of the trapped charges is shown in parenthesis. Reported error corresponds to the standard deviation of measurements from five devices per process.

Process	N_{eff} (10^{11} cm^{-2})	ΔN_{it} (10^{11} cm^{-2})
O	(−)54.9 ± 2.7	…
N	(−)52.3 ± 4.3	…
O + H	(−)3.9 ± 1.2	(−)10.2 ± 0.25
N + H	(+)9.0 ± 1.2	(−)1.14 ± 0.01

The effective charge densities (N_{eff}) are calculated by the shift between the experimental and ideal flatband voltages

Flat Band Voltage



- At the maximum slope of the left flank of the first derivative of the $1/(C_{hf})^2$ curve occurs at V_{FB}

CV Hysteresis Measurement

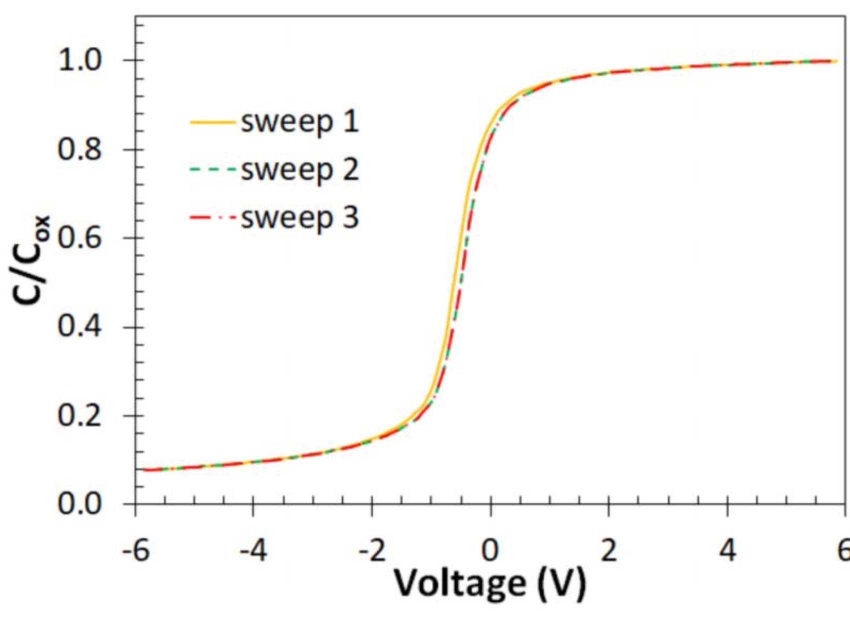
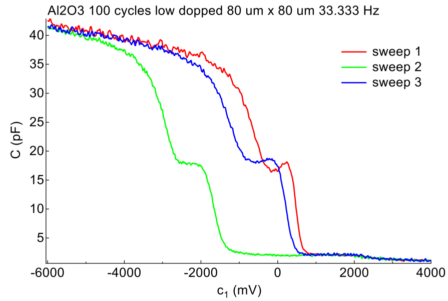


FIG. 3. CV hysteresis measured for Al_2O_3/4H-SiC MOS capacitor fabricated with process N + H. Three consecutive measurements were performed, sweep 1: depletion to accumulation, sweep 2: accumulation to depletion, and sweep 3: depletion to accumulation.



Sweep 1: depletion to accumulation
Sweep 2: accumulation to depletion
Sweep 3: depletion to accumulation

Shift due to energetically deep interface traps become filled with electrons during the first weep and do not emit during subsequent measurements

Dielectric Leakage

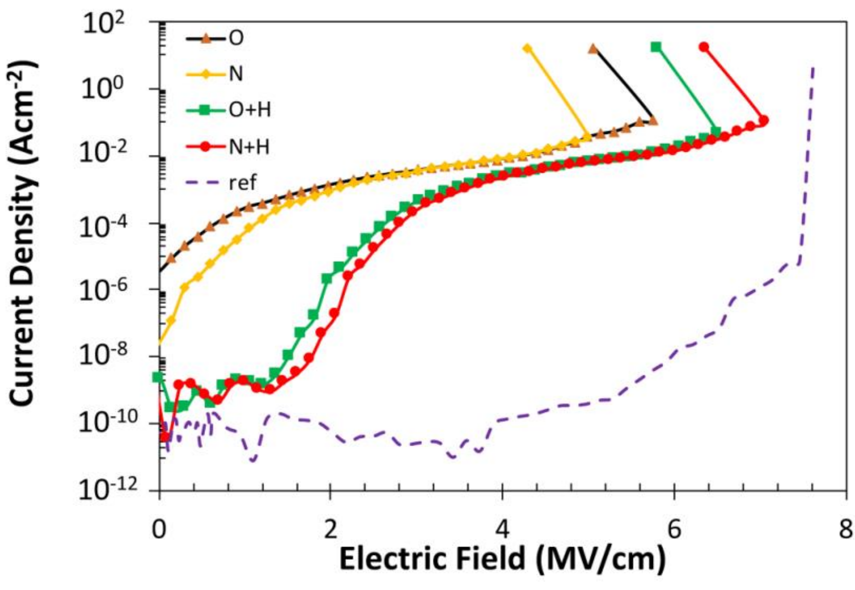


FIG. 4. Room temperature dielectric leakage current in Al_2O_3/4H-SiC MOS capacitors prepared with different surface treatments compared to NO annealed SiO_2/4H-SiC MOS capacitor (ref). The labeling of the samples is described in Table I and in the text.

Dominant leakage currents are likely due to trap-assisted tunneling mediated by near-interface traps

Conclusion

- Introducing N for the deposition of the dielectric is an advantage, it passivates the surface and enables the formation of high-quality interface between SiC and deposited dielectric
- Hydrogen annealing most effective when performed on sub nm SiON layers formed on 4H-SiC surfaces by nitric oxide annealing
- Surface nitridation and subsequent hydrogen annealing work in an additive manner

- Gate leakage of Al2O3 was significantly poorer than with SiO_2 , needs to be overcome